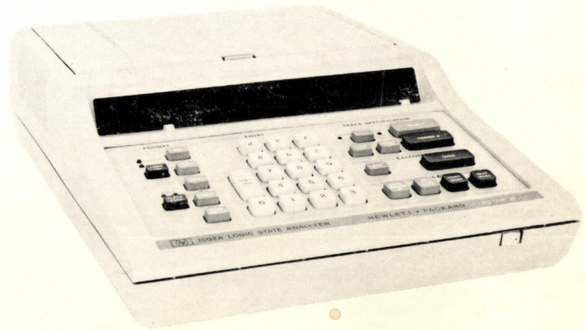
HP1602A

HP 1602A

1602A LOGIC STATE ANALYZER

OPERATING AND SERVICE MANUAL

1602A
LOGIC STATE ANALYZER



HEWLETT hp PACKARD

HP 1602A

01602-90902

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01602-90902

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OPERATING AND SERVICE MANUAL 01602-90902

CERTIFICATION

Hewlett-Packard Company certifies that this instrument met its published specifications at the time of shipment from the factory. Hewlett-Packard Company further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY AND ASSISTANCE

This Hewlett-Packard product is warranted against defects in materials and workmanship for a period of one year from the date of shipment. Hewlett-Packard will, at its option, repair or replace products which prove to be defective during the warranty period provided they are returned to Hewlett-Packard, and provided the preventive maintenance procedures in this manual are followed. Repairs necessitated by misuse of the product are not covered by this warranty. NO OTHER WARRANTIES ARE EXPRESSED OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANT-ABILITY AND FITNESS FOR A PARTICULAR PURPOSE. HEWLETT-PACKARD IS NOT LIABLE FOR CONSEQUENTIAL DAMAGES.

Service contracts or customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

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OPERATING AND SERVICE MANUAL

MODEL 1602A
LOGIC STATE ANALYZER

SERIAL NUMBERS

This manual applies directly to instruments with serial numbers prefixed **1717A.**

Manual Part Number 01602-90902
Microfiche Part No. 01602-90802

PRINTED: MARCH 1978

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

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Figure 1-1. Model 1602A Logic State Analyzer

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This Operating and Service Manual contains information required to install, operate, test, and service the HP Model 1602A Logic State Analyzer.

1-3. SPECIFICATIONS.

1-4. Instrument specifications are listed in table 1-1. These specifications are the performance standards or limits against which the instrument is tested. Table 1-2 lists supplemental characteristics. Supplemental characteristics are not specifications but are typical characteristics included as additional information for the user.

1-5. INSTRUMENTS COVERED BY THIS MANUAL.

1-6. Attached to the instrument is a serial number tag. The serial number is in the form: 0000A00000. It is in two parts; the first four digits and the letter are the serial prefix and the last five digits are the suffix. The prefix is the same for all identical instruments. The suffix, however, is assigned sequentially and is different for each instrument. The contents of this manual apply to instruments with the serial number prefix(es) listed under SERIAL NUMBERS on the title page.

1-7. An instrument manufactured after the printing of this manual may have a serial number prefix that is not listed on the title page. This unlisted serial number prefix indicates the instrument is different from those described in this manual. The manual for this newer instrument is accompanied by a Manual Changes supplement. This supplement contains "change information" that explains how to adapt the manual to the newer instrument.

1-8. In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard.

1-9. For information concerning a serial number prefix that is not listed on the title page or in the Manual Change supplement, contact your nearest Hewlett-Packard office.

Table 1-1. Specifications

CLOCK, DATA, AND CLOCK QUALIFIER PROBE INPUTS

REPETITION RATE: 10-MHz maximum.
INPUT LOAD: one low-power Schottky gate (<400 μA source).
INPUT THRESHOLD: TTL, fixed at approximately 1.5 V.
MAXIMUM INPUT: <+5.5 V.
MINIMUM INPUT
Level: >—0.5 V.
Swing: from ≤+0.4 V (LOW) to ≥+2.4 V (HIGH).
CLOCK PULSE WIDTH: ≥25 ns at threshold.
SETUP TIME: (time data must be present at 1602A probe input before clock transition) 35 ns at threshold.
HOLD TIME: (time data must be present at 1602A probe input after clock transition) 0 ns.

TRIGGER QUALIFIER AND CLOCK QUALIFIER INPUTS (REAR PANEL).

INPUT LOAD: 8 mA max source.
MAXIMUM INPUT: <+5.5 V.
MINIMUM INPUT
Level: >—0.5 V.
Swing: from ≤+0.4 V (LOW) to ≥+2.5 V (HIGH).
SETUP TIME: time data must be present before clock transition, 40 ns with Model 10250A probe, 10 ns without probe.
HOLD TIME: time data must be present after a clock transition, 15 ns with 10250A probe, 30 ns without probe.

TRIGGER AND TRACE POINT OUTPUTS

High: ≥2 V into 50Ω.
Low: ≤0.4 V into 50Ω.
PULSE DURATION (WIDTH)
Trigger: high for approximately one clock period.
Trace Point: sets low when Trace key is pressed, returns high when the Trace specification is met.

DELAY FROM INPUT CLOCK: <150 ns.

1-10. DESCRIPTION.

1-11. The Model 1602A keyboard-controlled Logic State Analyzer is intended for use in the design and troubleshooting of digital systems. The 16-bit wide, 64-word deep memory operates at clock speeds to 10 MHz and allows the instrument to capture virtually any 64-word sequence in a system. The data may be registered with versatile pattern recognition trigger and digital delay. Measurements of system activity are displayed on the 1602A LED readout in hexadecimal, decimal, octal, or binary format, which eliminates the need for base conversions by the operator. Keyboard entry of the desired trigger is in the same base as selected for the display.

1-12. The 1602A probe is a single pod containing all 16 data lines, clock, clock qualifier, and ground. At the front of the pod is a standard edge connector which allows the operator to quickly move the probe from one test point to another. Probe input threshold is TTL.

1-13. The Model 1602A has two rear panel TTL qualifier inputs: clock-qualifier and trigger-qualifier inputs are designed to be fully compatible with the Model 10250A "And" Gate Trigger Probe.

1-14. OPTIONS.

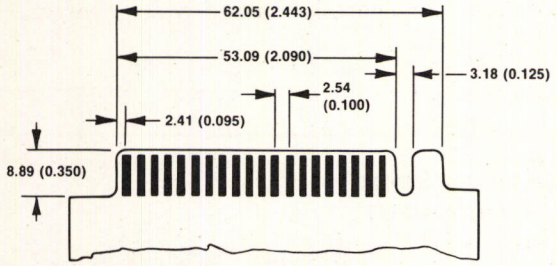
1-15. Standard options are modifications installed on HP instruments at the factory and are available on request. The following option is available for the 1602A:

OPTION 001: This option adapts the 1602A for use in a Hewlett-Packard Interface Bus (HP-IB) system. The

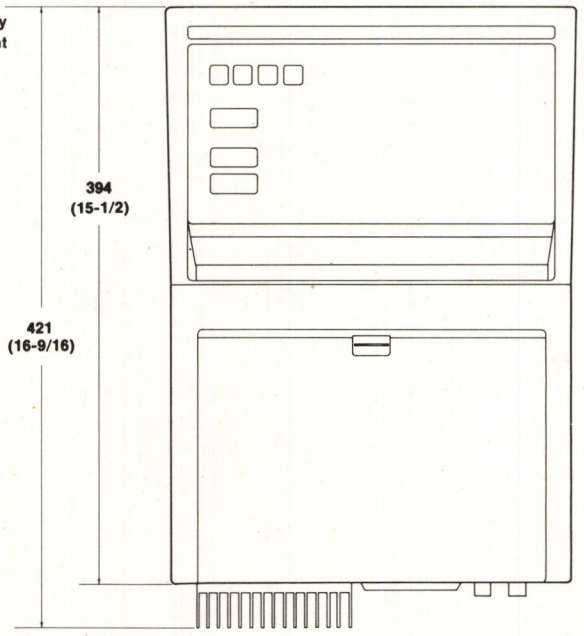
Table 1-2. Supplemental Characteristics

POWER REQUIREMENTS: 100, 120, 220, or 240 Vac; —10%, +5%; 48 to 66 Hz; 50 VA max.
DIMENSIONS: see outline drawings.
WEIGHT: net, 4.5 kg (10 lb).
OPERATING ENVIRONMENT
Temperature: 0°C to +55°C.
Humidity: up to 95% relative humidity at +40°C.
Altitude: to 4600 m (15 000 ft).
Vibration: vibrated in three planes for 15 minutes each with 0.38 mm (0.015 in.) excursions, 10 to 55 Hz.

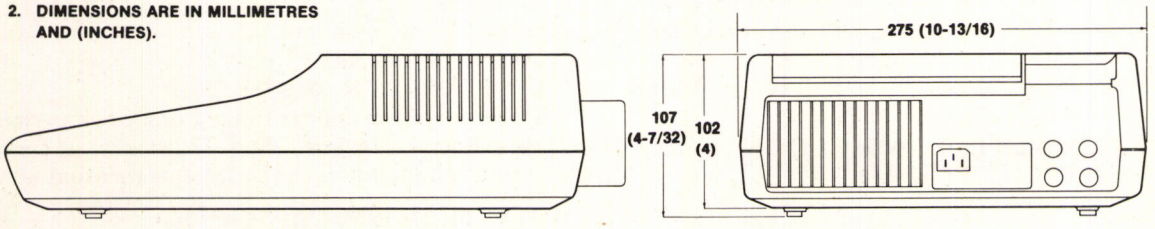
PROBE INTERFACE
The probe interface is a standard, two row, edge connector which may easily be added to instruments during development, providing convenient test points for production and field service requirements.



Notes
Dimensions in millimetres and (inches)
PC Board is 1.57 mm (0.062 in) thick.
Dimension Tolerance = 0.13 (0.005)



NOTES:
1. DIMENSIONS ARE FOR GENERAL INFORMATION ONLY. IF DIMENSIONS ARE REQUIRED FOR BUILDING SPECIAL ENCLOSURES, CONTACT YOUR HP FIELD ENGINEER.
2. DIMENSIONS ARE IN MILLIMETRES AND (INCHES).



HP-IB (see table 1-3) is compatible with IEEE Standard 488-1975, "Digital Interface for Programmable Instrumentation." The 1602A Option 001 can receive commands via HP-IB that simulate front-panel key entries. These commands cause the 1602A to assume a measurement configuration, execute Trace or Trace Events, and configure itself to transmit measurement results to other instruments on HP-IB. A field-installable kit (HP Part No. 10059A) is available which allows a standard 1602A to be modified for Option 001 capability.

HP-IB Response Times are as follows:

(1) Commands (ATN LO) are processed with approximately 1 μs delay.
(2) With 1602A addressed to talk/listen and ATN HI, message rates may be limited by 1602A software dependent delays to approximately 200 to 1000 bytes/second.

1-16. ACCESSORIES SUPPLIED.

1-17. The following accessories are supplied with the 1602A:

One AC Power Cord, HP Part No. 8120-1378.
One 0.25 AT (slow-blow) fuse, HP Part No. 2110-0201 (for 220-240 Vac operation).
One Probe Wire-Adapter Assembly, HP Part No. 01602-62102. Plugs into the Data Probe and provides individual clock, data, and clock qualifier input leads with hook-type circuit probes.

1-18. ACCESSORIES AVAILABLE.

1-19. The following items are available for use with the 1602A:

Model 10050A HP-IB Connector/Adapter. Allows convenient connection to an HP-IB cable with either the Data Probe or with the HP-IB Test Probe (Model 10051A) for bus monitoring.
Model 10051A HP-IB Test Probe. Connects between the Data Probe and a Model 10050A to allow easier and more complete HP-IB monitoring.
Model 10250A TTL Trigger Probe. Connects to rear panel Trigger Qualifier or Clock Qualifier inputs and provides an additional four bits of qualification (each bit may be set HI, LO, or OFF).
Model 10060A Application Program for HP9825A calculator/1602A Opt 001.
Replacement Hook-type Circuit Probes (HP Part No. 10230-62101).
Convenience Connector Kit (HP Part No. 01602-68701). Consists of Probe Wire-Adapter Assembly without Circuit Probes.
Convenience Connector Kit (HP Part No. 01602-68702). Consists of Probe Wire-Adapter Assembly without Circuit Probes, Label, and Pin Adapter Wire Cables.

1-20. RECOMMENDED TEST EQUIPMENT.

1-21. Equipment required to test and maintain the 1602A is listed in table 1-4. Other equipment may be substituted if it meets or exceeds the critical specifications listed in the table.

Table 1-3. Model 1602A Option 001 – HP-IB Interface Capabilities

CODE	INTERFACE FUNCTION CAPABILITY
SH1	Source Handshake
AH1	Acceptor Handshake
T7	Talker (basic talker, talk only mode, unaddress to talk if addressed to listen)
L4	Listener (basic listener, unaddress to listen if addressed to talk)
SR0	No Service Request
RL1	Remote/Local
PP0	No Parallel Poll
DC0	No Device Clear
DT0	No Device Trigger
C0	No Controller
E1	Open-collector Bus Drivers

Table 1-4. Recommended Test Equipment

INSTRUMENT	CRITICAL SPECIFICATION	RECOMMENDED MODEL	*USE
Pulse Generator (2)	5 V output into 50Ω, External trigger, 0 to 35 ns delay	HP 8012B	P
Dual-channel Oscilloscope	100 MHz bandwidth	HP 1740A	P, T
Probe Test Source	16-bit binary counter	HP Part No. 5061-1254	P
Feedthrough Termination (2)	50Ω feedthrough	HP 10100C	P
BNC Adapter Tip	BNC-to-scope probe adapter	HP 10011B	P
BNC-to-alligator Clip Adapter (2)		HP Part No. 8120-1292	P
BNC Tee Connector (2)		HP Part No. 1250-0781	P
HP-IB Controller	IEEE 488-1975 Controller Capability (C1)	HP 9825A or HP 9830A	P (Opt 001)

*P=Performance Test; A=Adjustments; T=Troubleshooting

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section provides installation instructions for the Model 1602A Logic State Analyzer. Initial inspection, damage claims, preparation for use, and repacking for shipment procedures are also included.

2-3. INITIAL INSPECTION.

2-4. Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until contents of the shipment are checked and instrument performance tests are completed. Contents of the shipment should include all items listed in the "Accessories Supplied" paragraph in Section I. Procedures for checking instrument performance are given in Section IV. If shipment contents are incomplete, if there is mechanical damage, or if the instrument does not pass the Performance Test, notify the nearest Hewlett-Packard Office. If the shipping container is damaged, or the cushioning material shows signs of stress, notify the carrier as well as the Hewlett-Packard Office. The HP Office will arrange for repair or replacement at HP option without waiting for claim settlement.

2-5. PREPARATION FOR USE.

WARNING

Read the Safety Summary at the front of this manual before installing or operating the instrument.

2-6. POWER REQUIREMENTS. The 1602A requires a power source of 100, 120, 220, or 240 Vac ±10%, 48 to 66 Hz, single phase. Power consumption is 50 VA (maximum).

CAUTION

Instrument damage may result if the AC Line Selector Board is not positioned correctly for the input power source.

2-7. LINE VOLTAGE SELECTION. The instrument is normally set at the factory for 115/120-V operation. To operate the instrument from any other ac power source, proceed as follows:

a. Disconnect input power cable from instrument.

b. Slide plastic fuse cover to left side of ac power module.

c. Rotate FUSE PULL handle to left and remove fuse.

d. Remove AC Line Selector Board from ac power module.

e. Position AC Line Selector Board for proper operating voltage (see figure 2-1).

NOTE

Selected operating voltage will be displayed on top-left side of AC Line Selector Board when it is installed.

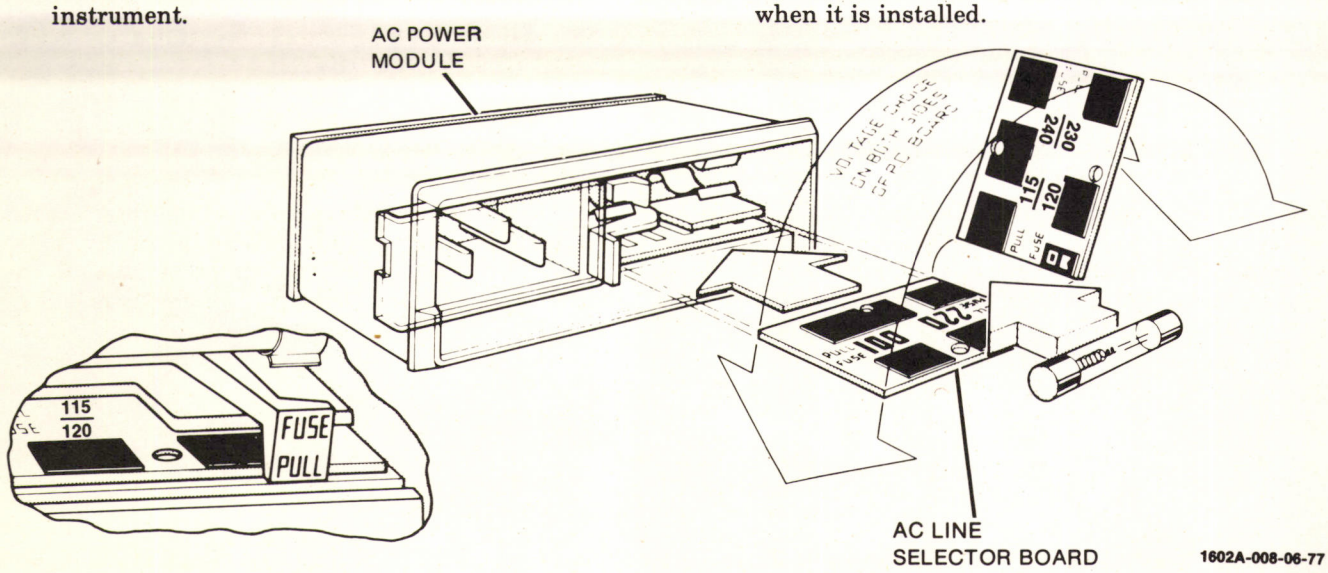


Figure 2-1. Line Voltage Selection

f. Push AC Line Selector Board firmly into ac power module slot.

g. Return FUSE PULL handle to normal position.

h. For 220- 240-V operation, install 0.25 AT (slow-blow) fuse, HP Part No. 2110-0201. For 100- 120-V operation, install 0.5 AT (slow-blow) fuse, HP Part No. 2110-0202.

i. Slide plastic fuse cover to right side of ac power module.

j. Connect power cable to instrument.

2-8. POWER CABLE. This instrument is equipped with a three-wire power cable. When connected to an appropriate ac power receptacle, this cable grounds the instrument chassis. The type of power cable plug shipped with each instrument depends on the country of destination. See figure 2-2 for the part numbers of available power cables with plug configurations as shown.

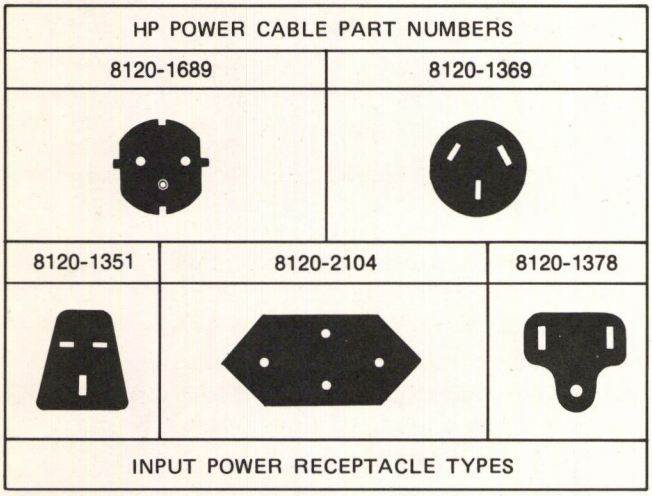


Figure 2-2. Power Cables Available

2-9. REPACKING FOR SHIPMENT.

2-10. If the instrument is to be shipped to a Hewlett-Packard Office for service or repair, attach a tag showing owner (with address), complete instrument serial number, and a description of the service required.

2-11. Use the original shipping carton and packing material. If the original packing material is not available, the Hewlett-Packard Office will provide information and recommendations on materials to use.

2-12. HP-IB ADDRESS SELECTION (OPTION 001 ONLY).

2-13. The "talk" and "listen" addresses for the 1602A Option 001 are selected by the ADDRESS SWITCH, a six-section switch on the rear panel. The five switches labeled A1 thru A5 are used to select the unique talk and listen address. They may be left at factory settings (01111) for talk and listen addresses, or they can be set to any alternate setting available. The sixth switch may be set to either TALK ONLY or to ADDRESSABLE. Talk only mode is used in systems without a controller. See figure 2-3 and table 2-1 for available address codes and corresponding switch settings.

NOTE

The 5-bit decimal code, consisting of bits A1 thru A5, is often used by controllers as a System Device Number for instruments.

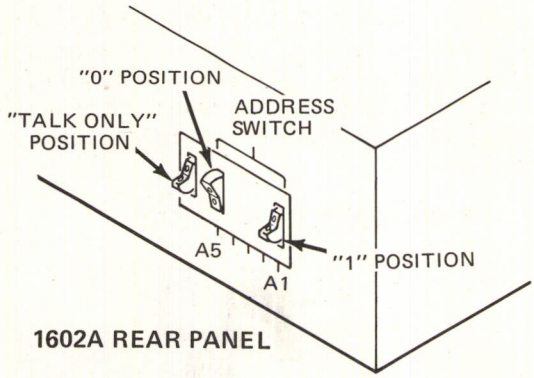


Figure 2-3. Address Switch Positions

2-14. HP-IB SYSTEM INTERFACE CONNECTIONS (OPTION 001 ONLY).

2-15. The 1602A is connected to the HP-IB by connecting an HP-IB interface cable to the 1602A rear-panel HP-IB connector (figure 2-4). As many as 15 instruments can be connected to the same interface bus. The maximum cable length that can be used is: (a) two meters (6.5 ft.) times the number of instruments connected; or (b) 20 meters (65.6 ft.), whichever is less.

Table 2-1. Address Codes

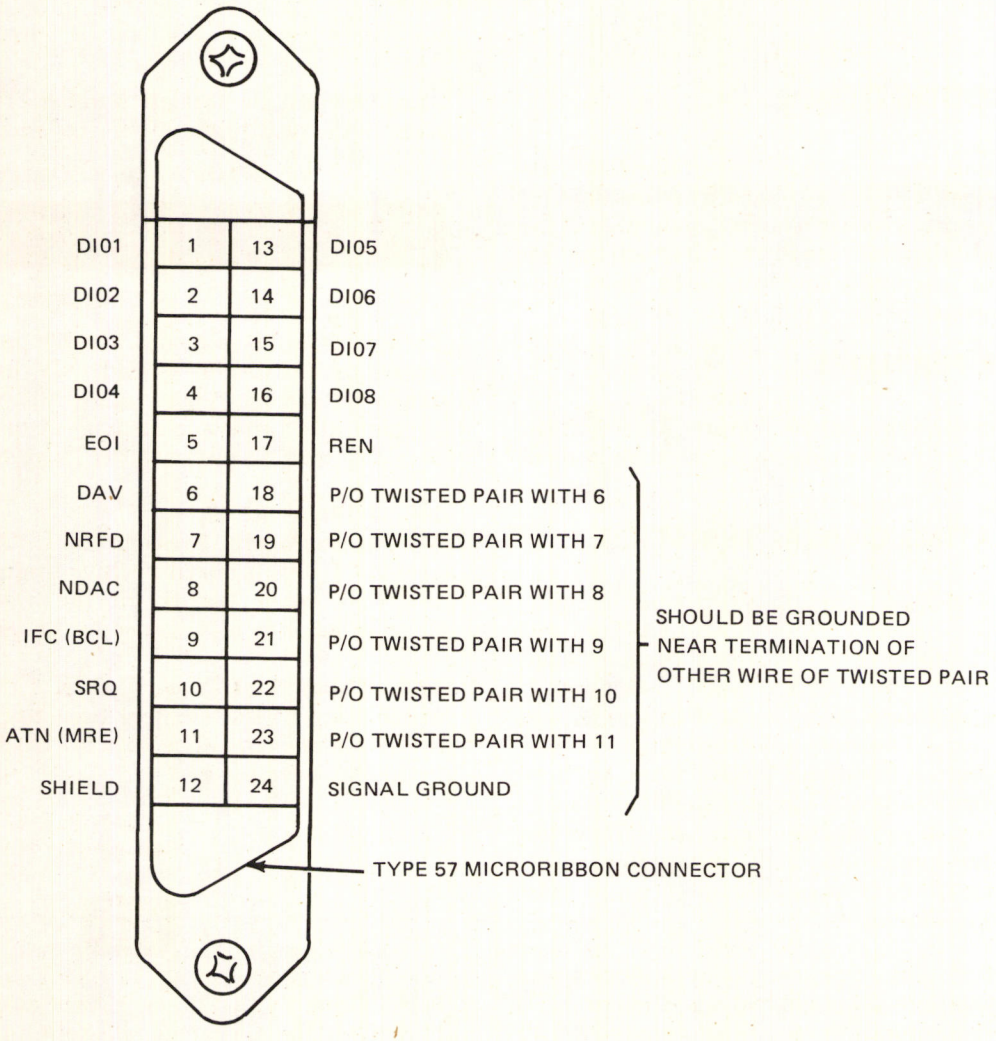
ASCII CODE CHARACTER		BINARY CODE							OCTAL CODE		5 BIT DECIMAL[3] EQUIVALENT
Listen Address	Talk Address	b_7[1]	b_6	A5 b_5	A4 b_4	A3 b_3	A2 b_2	A1 b_1	Listen	Talk	
SP	@			0	0	0	0	0	040	100	0
!	A			0	0	0	0	1	041	101	1
"	B			0	0	0	1	0	042	102	2
#	C			0	0	0	1	1	043	103	3
$	D			0	0	1	0	0	044	104	4
%	E			0	0	1	0	1	045	105	5
&	F			0	0	1	1	0	046	106	6
'	G			0	0	1	1	1	047	107	7
(	H			0	1	0	0	0	050	110	8
)	I			0	1	0	0	1	051	111	9
*	J			0	1	0	1	0	052	112	10
+	K			0	1	0	1	1	053	113	11
,	L			0	1	1	0	0	054	114	12
-	M			0	1	1	0	1	055	115	13
.	N			0	1	1	1	0	056	116	14
/	**O**			**0**	**1**	**1**	**1**	**1**[2]	**057**	**117**	**15**[2]
Ø	P			1	0	0	0	0	060	120	16
1	Q			1	0	0	0	1	061	121	17
2	R			1	0	0	1	0	062	122	18
3	S			1	0	0	1	1	063	123	19
4	T			1	0	1	0	0	064	124	20
5	U			1	0	1	0	1	065	125	21
6	V			1	0	1	1	0	066	126	22
7	W			1	0	1	1	1	067	127	23
8	X			1	1	0	0	0	070	130	24
9	Y			1	1	0	0	1	071	131	25
:	Z			1	1	0	1	0	072	132	26
;	[			1	1	0	1	1	073	133	27
<	\			1	1	1	0	0	074	134	28
=	]			1	1	1	0	1	075	135	29
>	~			1	1	1	1	0	076	136	30

[1]Only the first five bits of the binary code are listed. These bits (set by A7S1) are the same for both the TALK and LISTEN address. The sixth and seventh bits (controller originated and put on Bus DI06 and DI07 lines) determine whether the instrument is being addressed to TALK or LISTEN.

[2]1602A Opt. 001 factory preset address.

[3]Derived from the sum of the binary weighted value of the first five address bits.

Function	Bit 7	6
Talk	1	0
Listen	0	1



Mating Cables: HP 10631A, 0.9 meters (3 ft.); HP 10631B, 1.8 meters (6 ft.); HP 10631C, 3.7 meters (12 ft.).

Bus Mnemonics:

DI01-DI08	Data Input/Output
EOI	End or Identify
DAV	Data Valid
NRFD	Not Ready for Data
NDAC	Data Not Accepted
IFC	Interface Clear
SRQ	Service Request
ATN	Attention
REN	Remote Enable

Figure 2-4. Hewlett-Packard Interface Bus Connector

SECTION III

OPERATION

3-1. INTRODUCTION.

3-2. This section provides operating information, explains functions of 1602A controls, connectors, and indicators and describes measurement capabilities of the instrument. Abbreviated operating instructions are also provided on a separate card (inside the instrument storage compartment).

3-3. PANEL FEATURES.

3-4. 1602A keyboard and panel features are described in figure 3-1. Description numbers match the numbers on the illustration.

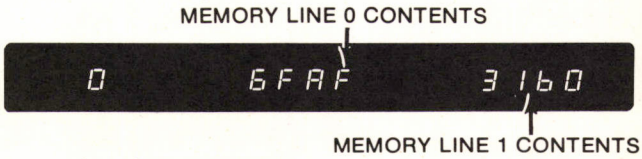
3-5. OPERATING CHARACTERISTICS.

3-6. PROBE. The 1602A probe is a single pod containing all 16 data lines and clock, clock qualifier, and ground lines. The front of the probe is a standard edge connector. One connector with individual clock, ground, clock qualifier, and data probe leads with tips is supplied with the probe. The probe edge connector makes it easy to build special interfaces for a system, such as permanently wired leads to IC clips for in-circuit testing of ICs or to any other special connectors. When the system under test has standard edge connectors, point-to-point probing (16 data lines at a time) can be very useful in troubleshooting.

3-7. DISPLAY. Format, Trigger or Delay specification, or acquired data are displayed or an 18-digit LED readout. All hexadecimal characters are generated with the seven segment LED display by using both lowercase and uppercase letters.

Be careful not to confuse the lowercase b with numeric 6.

With decimal, hexadecimal, and octal codes, two acquired data words are displayed on the LEDs. The left word is the current word at the memory location identified by the far left number. The word on the right is the next higher numbered memory location.

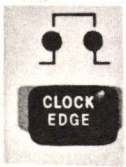


For binary or mixed modes where more than six LEDs are required to display a word, only the current word is displayed. Display keys allow the operator to roll through all 64 words in memory or to position the display at a word in any memory location.

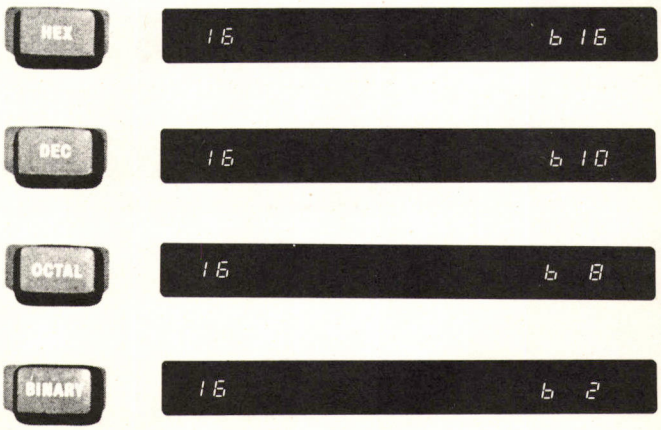
3-8. FORMAT KEYS.

3-9. Logic Polarity. Pressing the LOGIC POL key toggles the 1602A between positive (high true) and negative (low true) polarity for the system under test. Selected polarity is indicated by LEDs above the key.

3-10. Clock Edge. The CLOCK EDGE key selects which edge of the clock is used to strobe data into the 1602A memory. The selected clock edge is shown by LEDs above the key.



3-11. Code Keys. The code keys select the code displayed on the LED readout. Selecting HEX formats the display in base 16 (b 16), and the data display includes alphanumerics 0 through F. For decimal (b 10), the data display contains numerics 0 through 9; in octal (b 8), 0-7; and in binary (b 2), 0 and 1.



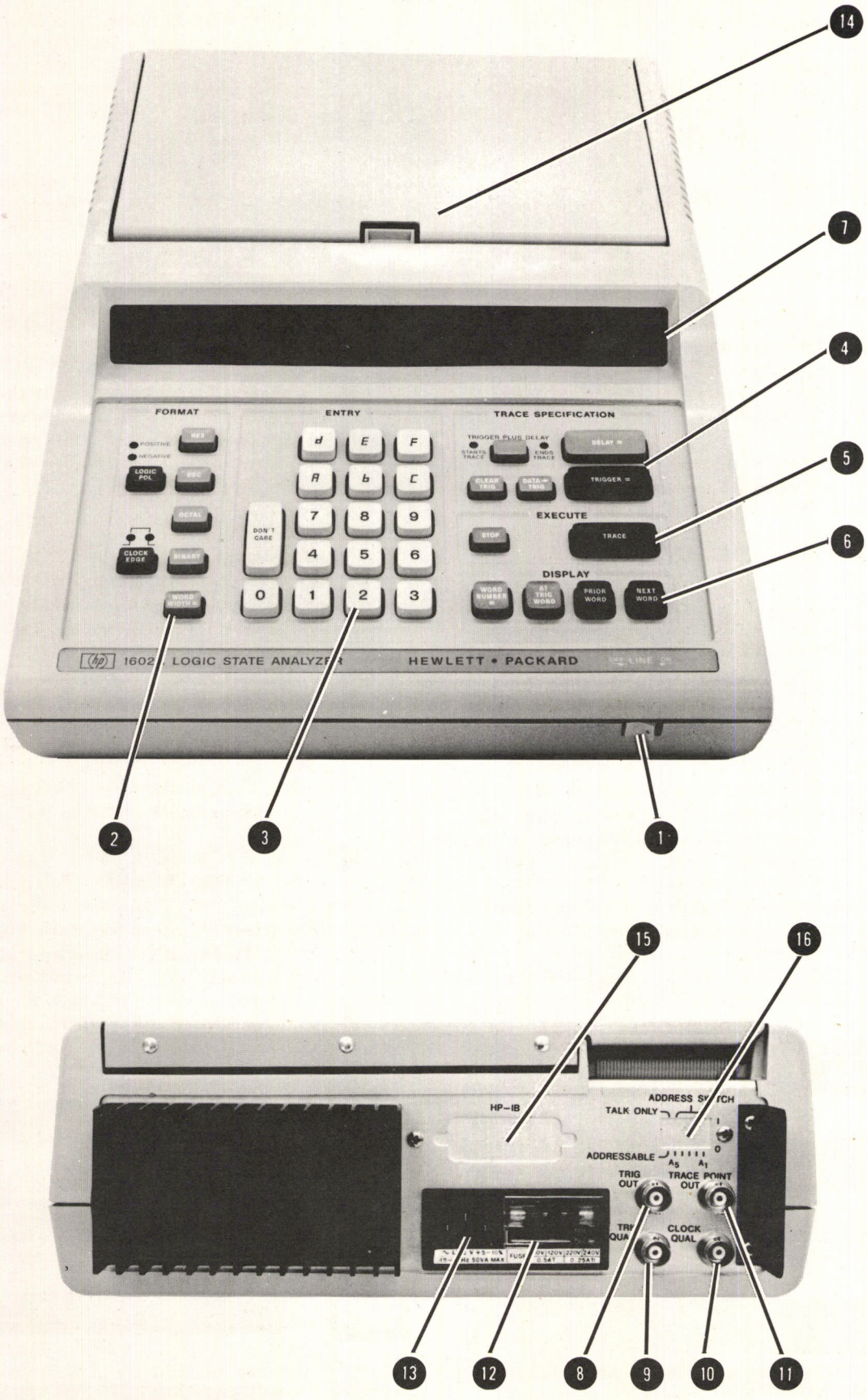


Figure 3-1. 1602A Controls, Connectors, and Indicators

1 **LINE.** Line Power Switch.

2 **FORMAT KEYS.**
LOGIC POL. Selects positive (high true) or negative (low true) polarity for data inputs. LEDs above key indicate selected polarity.

CLOCK EDGE. Selects which edge of clock strobes data into 1602A memory. LEDs above key indicate selected edge.

CODE KEYS. Select code (number base) displayed on LED readout (hexadecimal, decimal, octal, binary).
WORD WIDTH=. Enables number of bits in trigger and displayed word (from 2 to 16) to be entered in decimal format through entry keys.

3 **ENTRY KEYS.** Used to enter all format, trace specification, and display control data into 1602A. Trigger field requires that data be entered in format selected by code keys. All other fields require decimal format. Alpha keys also provide special functions (refer to Operating Characteristics).

4 **TRACE SPECIFICATION KEYS.**
TRIGGER PLUS DELAY. Selects whether trace starts or ends when trigger plus delay conditions are met. LEDs indicate selection.

DELAY=. Enables number of clocks or events to be delayed (from 0 to 65 535) to be entered in decimal format using entry keys. When pressed, current delay is displayed.

TRIGGER=. Enables trigger word to be entered in selected code using entry keys. Trigger field size is consistent with selected code base and word width. When pressed, current trigger word is displayed.

DATA→TRIG. Enters current displayed word into trigger register for use as trigger word.

CLEAR TRIG. Enters all "don't cares" into trigger register.

5 **EXECUTE KEYS.**
TRACE. Starts measurement. Loads memory with 64 words of data beginning (or ending) when the trace specification is met.

STOP. Halts trace and forces 1602A into display mode. Memory locations not written into are displayed as "don't cares" (dashes).

6 **DISPLAY KEYS.**
NEXT WORD. Moves word in next higher memory location into display. If held down, data rolls through display at 3 word per-second rate.

PRIOR WORD. Same as next word, except decrements memory locations.

WORD NUMBER=. Enables addressing any memory location (0 to 63) in decimal format through entry keys.

AT TRIG WORD. Repositions display to memory location containing trigger word if word is contained in memory.

7 **DISPLAY.** 18 character, seven-segment LED display.

8 **TRIG OUT.** BNC output providing positive-going pulse each time trigger plus delay specification is satisfied. Signal returns to low state one clock period later. Trigger is provided each time trigger plus delay specification is satisfied, whether or not 1602A is performing a trace. (High level >2 V, low level <0.4 V into 50Ω.)

9 **TRIG QUAL.** BNC input used as additional trace point qualifier in parallel with 16 data lines. When low, 1602A ignores Trigger words. When high, 1602A is allowed to recognize Trigger words. Input is pulled high when disconnected.

10 **CLOCK QUAL.** BNC input used to control which clocks are allowed to strobe data into 1602A memory. When low, trigger recognition, delay, and memory loading are inhibited; when high, clocks are enabled. Input is pulled high when disconnected.

11 **TRACE POINT OUT.** BNC output occurring once per trace. Normally high signal drops to low level when TRACE key is pressed. Signal returns to high level when trace specification (trigger plus delay) is satisfied. Signal remains high until TRACE key is pressed again.

12 **FUSE AND LINE SELECTOR.** Selects line operating voltage (100, 120, 220, or 240 Vac). Refer to Section II.

13 **LINE INPUT CONNECTOR.** Power cable connector.

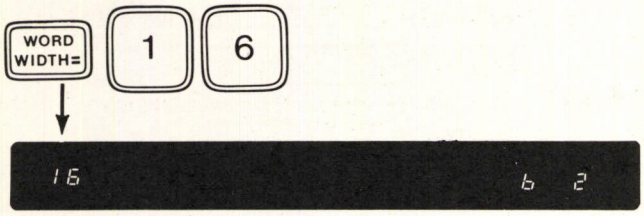
14 **STORAGE COMPARTMENT.** For storing probe and accessories.

15 **HP-IB Connector Receptacle.** For connecting 1602A to HP-IB (Option 001 only).

16 **HP-IB Address, Talk Only/Addressable Switch.** Sets 1602A HP-IB address for talking and listening via HP-IB, and places 1602A in Talk Only or Addressable mode. Factory set to address 01111 (15_{10}) and Addressable. (Option 001 only).

3-12. Word Width. The WORD WIDTH= key selects the number of bits (from 2 to 16) in the displayed word. The number of bits is entered in decimal format through the Entry keys.

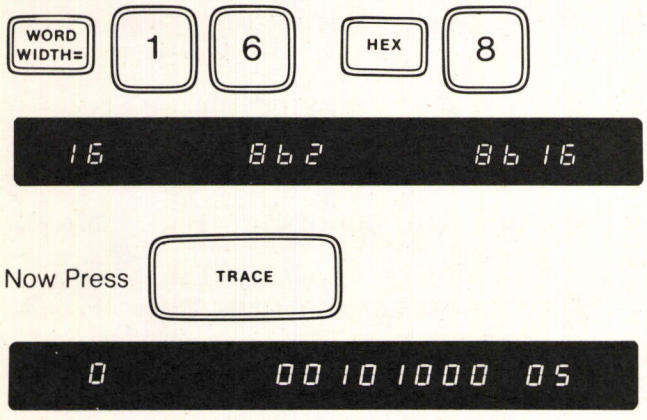
Example:



The selected bits are right-justified and always start at bit "0." Unused bits are blanked on the display. Selecting a 12-bit word displays inputs 0 through 11 and blanks bits 12-15. The 1602A memory contains all 16 input bits, so the display format may be changed after a run is complete if desired. All unused bits are "don't cares" in the trigger specification.

3-13. MIXED FORMAT. A mixed format of binary and any other base can be displayed. Press WORD WIDTH= and enter the number of bits desired in the word. Then press a high base code key such as HEX, and enter the number of bits desired in that code. The 1602A automatically puts the remainder of input bits in binary. Least significant bits on the display are formatted in the higher base code. Refer to paragraphs 3-19 and 3-20 for details on mixed format trigger specification.

Example:



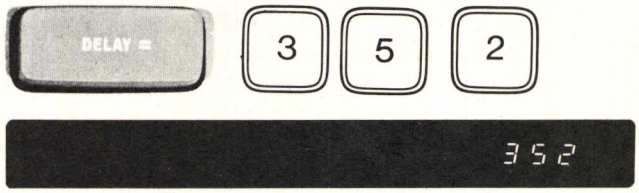
3-14. ENTRY KEYS. These keys are used to enter all format, trace specification, and display control data into the 1602A. Format of the data entry is defined by the field opened. The TRIGGER= field requires data to be entered in the format defined by the code key. Delay fields, word width, and word number are all entered in decimal format. The alpha keys are also used for special functions defined later in this section.

3-15. TRACE SPECIFICATION. The function of the five trace specification keys is to define the position of the 1602A memory window within the system under test activity (see the 1602A trace model shown in figure 3-2).

3-16. Trigger Plus Delay. This switch selects whether the trace starts or ends when the trigger and delay conditions are met. The selected mode is indicated by LEDs on either side of the key.

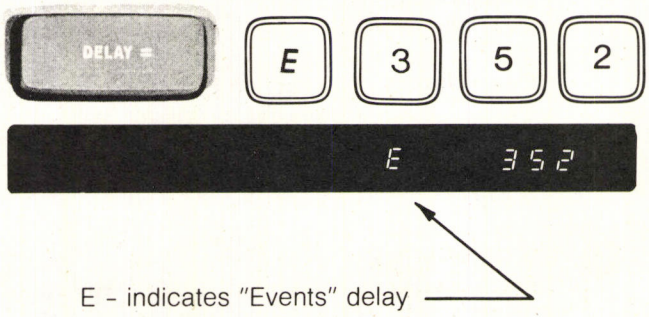
3-17. Delay. Pressing the DELAY= key opens the delay data field. Clock delays from 0 to 65 535 can then be entered in decimal format using the entry keys.

Example:



3-18. In addition to clock delay, the 1602A can also delay by trigger events. This mode is enabled by pressing DELAY= followed by E and then the desired number of events from 0 to 65 535. N + 1 trigger events then satisfy the conditions of the trace specification.

Example:



This mode makes it possible to look deep into loops, view the N + 1 occurrence of an input or output event, or sample activity in a program at predetermined points.

3-19. Trigger. The TRIGGER= key opens a trigger field at the right of the display. Size of the trigger field is consistent with the code base and word width selected. A dash represents the position of a single "don't care" character in the field. For a word width of

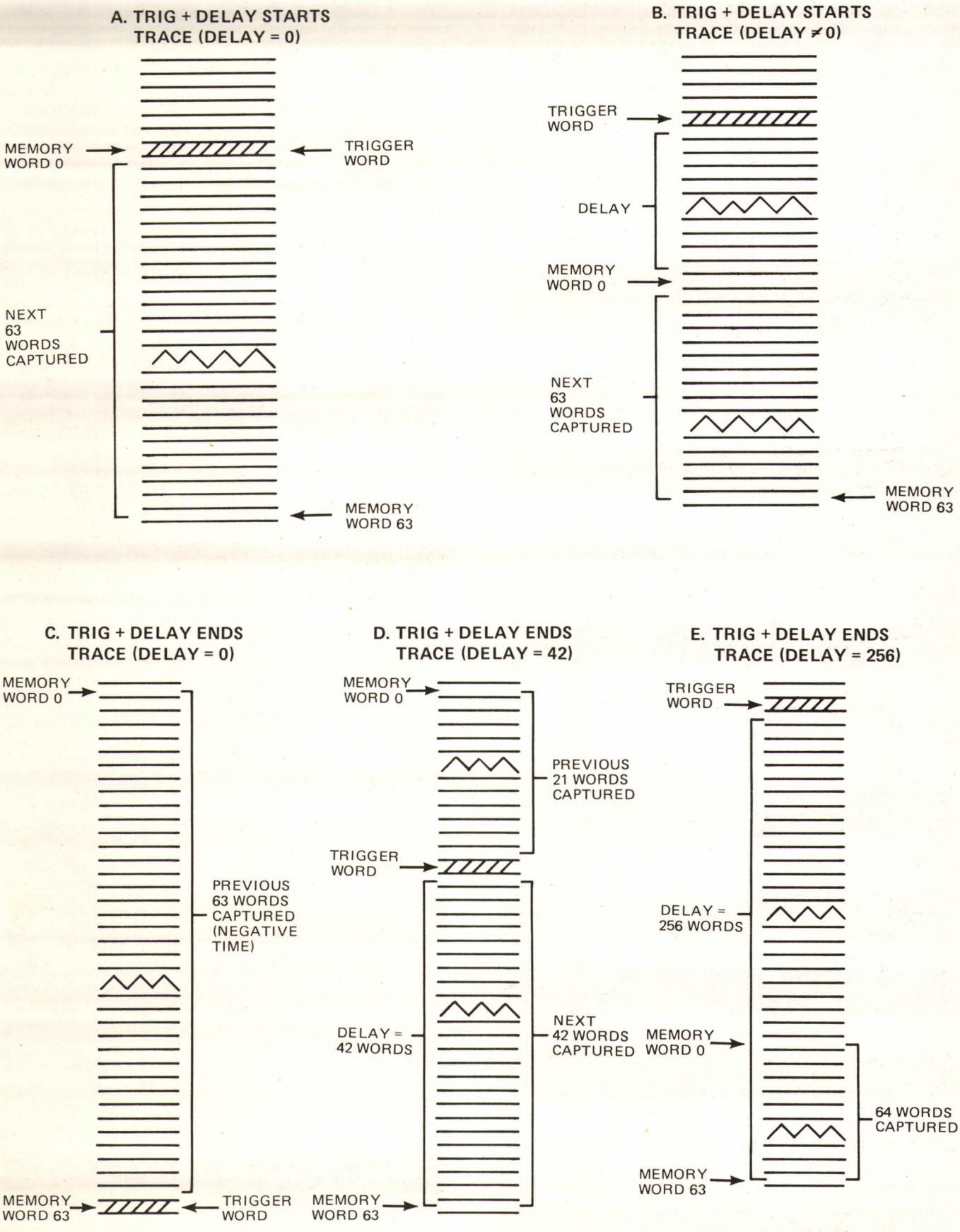
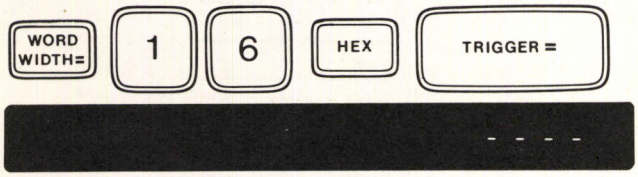
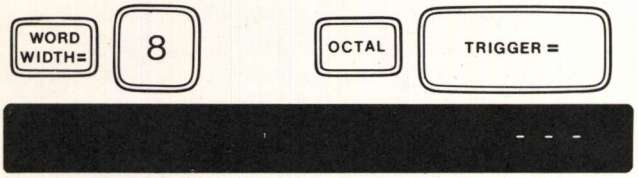


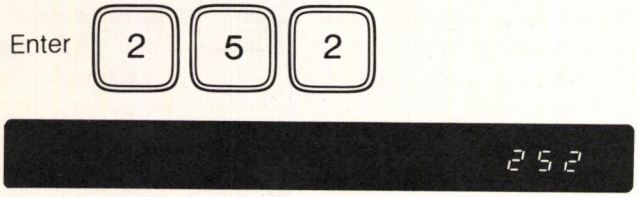
Figure 3-2. 1602A Trace Models

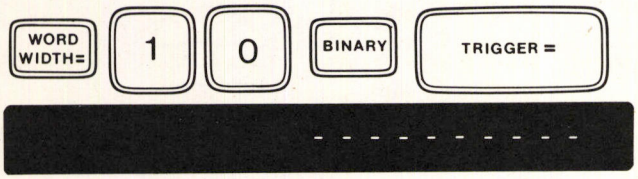
16 bits in hex code, the trigger field is four characters wide. With octal code and a word width of 7 bits, 3 spaces are opened in the trigger field. A binary word width of 10 has a trigger field of 10 characters. If a trigger word has been previously stored, it is displayed when TRIGGER= is pressed. Subsequent entries will change the trigger word.

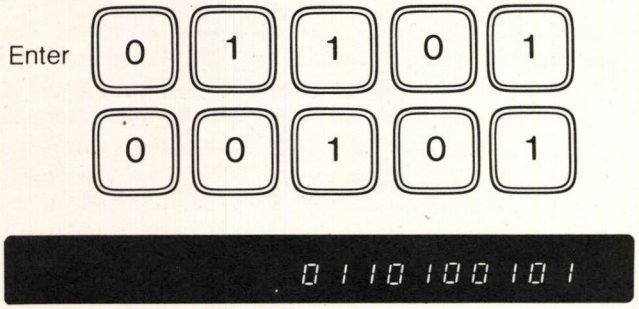
Examples:











3-20. Trigger data must be entered in the format selected for display. In hex format, alphanumerics 0 through F may be used; in decimal, numerics 0-9; in octal, numerics 0-7; and in binary, 0 and 1. For mixed format modes, press TRIGGER= and enter the part of the trigger in the higher base. Then press BINARY and enter the remaining characters in 1's and 0's.

Example:

The DON'T CARE key may be used in any format. "Don't cares" are shown as dashes on the display.

3-21. Data→Trig. The DATA→TRIG key moves the currently displayed word in memory into the trigger register. This key allows paging through program flow in blocks of 64 by transferring word number 63 (in STARTS TRACE mode) to the trigger register and retracing. Repeating the process pages through program flow in 64 word blocks very rapidly.

3-22. Clear Trigger. The CLEAR TRIG key puts all "don't cares" in the trigger word.

3-23. EXECUTE KEYS.

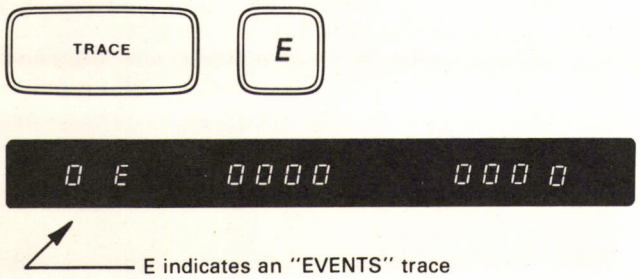
3-24. Trace. When the TRACE key is pressed, the 1602A starts searching for the trigger point. While the search is in progress, the TRACE light in the upper-right corner of the display remains on as a status indication. When the trace is completed (Trigger word plus Delay specification satisfied), the unit automatically displays the current word. With higher base codes, two words are displayed on the LEDs. For binary or mixed modes where more than six LEDs are required to display a word, only one word is displayed.

Example:

Memory Location	Current Word	Next Word

3-25. Trace Events. Pressing TRACE followed by E places the 1602A in a trace events mode. In this mode, the 1602A captures only those words that satisfy the trace specification (trigger word plus delay). For example, by triggering on an output port address or strobe signal and adding a small delay, sequential output data can be viewed; or by triggering on a jump instruction and delaying a few clocks, the jump to addresses can be captured.

Example:



3-26. Trace Continuous. Pressing TRACE followed by C places the 1602A in a trace continuous mode. The 1602A then repetitively samples at a maximum 10 Hz rate and displays the acquired data. This is useful in monitoring a point in the data stream for changes or for checking the input lines to verify that all are toggling.

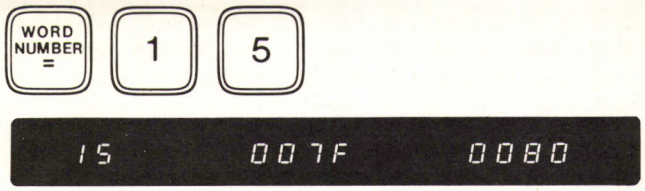
3-27. Stop. The STOP key halts the trace and forces the 1602A into a display mode. All data collected when STOP is pressed is stored in memory. Memory locations that were not written into during the last trace are displayed as "don't cares" (dashes).

3-28. DISPLAY KEYS.

3-29. Next Word. Each time the NEXT WORD key is pressed, the word in the next higher memory location is moved into the display. If the key is held down, data will roll through the display at approximately 3 words per second.

3-30. Prior Word. The PRIOR WORD key functions in the same manner as the NEXT WORD key but moves the word in the next lower memory location into the display.

3-31. Word Number. The WORD NUMBER= key permits addressing any of the 64 memory locations by entering its decimal location number. For example, pressing WORD NUMBER= and entering 15 immediately displays the data stored at memory location 15.



3-32. At Trigger Word. Pressing AT TRIGGER WORD repositions the display to the memory location that contains the trigger word, if it is stored in memory.

NOTE

Pressing TRACE does not automatically reset the display to memory location "0." Repeated tracings can be made on the last memory location selected for viewing. If a parameter is changed that affects the trace specification (delay, trigger word, clock slope, etc.), the display automatically resets to the trigger word or location "0," whichever is appropriate.

3-33. REAR-PANEL CONNECTORS.

3-34. Trigger Qualifier. The TRIG QUAL input can be used as an additional trigger word in parallel with the 16 data lines. When held low, the 1602A cannot recognize Trigger words. When held high, Trigger words can be recognized. The input is pulled high when disconnected. This input requires TTL levels.

3-35. Clock Qualifier. The CLOCK QUAL input controls which clocks are allowed to strobe data into the 1602A memory. When low, trigger recognition, delay, and memory loading are inhibited. When high, the 1602A is qualified, allowing data to be strobed into memory. The CLOCK QUAL input is pulled high when disconnected. This input requires TTL levels.

NOTE

The clock qualifier input on the probe pod functions the same as the rear-panel clock qualifier input.

3-36. Rear Panel Qualifier Timing. The 1602A clock signal must occur at least 10 ns after the qualifier line goes high (setup time), and the line must remain high for at least 30 ns after the clock occurs (hold time).

3-37. Trigger Output. The TRIG OUT connector provides a positive-going edge each time an event (trigger plus delay) is detected, returning to a low level approximately one clock period later. If the program is nonrepeating, there will only be one pulse from the TRIG OUT connector. If the monitored program is looping, a pulse is generated each time the trigger pattern (plus delay) is recognized. A low level on this output is <0.4 V and a high level is >2 V into 50Ω. This output is produced whether or not the TRACE key is pressed.

3-38. Trace Point Output. The TRACE POINT OUT signal occurs once per trace. The output is normally high and drops to a low level when the TRACE key is pressed. It remains low until the trace specification (trigger plus delay) is met, and at this time it goes high. The signal remains high until TRACE is pressed again. This output can be used with storage oscilloscopes to view the exact data stored in the analyzer's memory or for slaving other state analyzers to the 1602A.

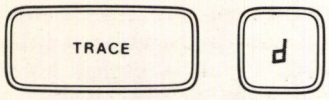
3-39. Trigger Timing. The positive-going edge of both the TRIG OUT and TRACE POINT OUT signals are virtually simultaneous. The signals lag the input clocks by approximately 150 ns. This may result in the leading edge of a data waveform presented to a scope occurring before the scope is triggered. This can be compensated for by triggering the 1602A on the data occurring one clock earlier than the state to be viewed on the oscilloscope.

3-40. 32-BIT SYSTEM. Two 1602As can be paralled to provide 32-bit operation as follows:

a. Connect TRACE POINT OUT from master unit to TRIG QUAL input of slave unit.

b. Set TRIGGER= on slave unit to "don't care." This allows master unit to control data collection point on both units.

c. To start data collection sequence, press TRACE then d on master unit. This holds master unit in search mode (forces Trace Point Output LO) but does not allow it to recognize a trigger.



d. Press TRACE on slave unit when desired, and then press TRACE on master unit. Both instruments will now gather data.

NOTE

The upper clock speed for 32-bit operation is 6 MHz. This is due to the 150 ns delay from the input clock to the trigger output. When the clock period becomes approximately equal to the delay, the slave unit may trigger erratically or not at all. Also, the data in the slave unit is delayed one clock from that in the master unit. In some systems the one clock delay between the two 1602As can be compensated for by operating the master unit on the leading edge of the clock and the slave on the trailing edge of the clock. This requires a clock width >160 ns and the data must be valid on both clock edges.

3-41. MESSAGE CODES.

3-42. The following messages are displayed when an operator error is made (such as attempting to enter a hex character in a binary data field) or when an instrument malfunction is detected. Messages also indicate operating status of the 1602A.

E1: Indicates that characters in the stored trigger contain a mixture of defined and "don't care" states. This can occur when a trigger word is entered in one code and then the format is changed to a different code. For example, if 11 - - is entered in binary and then hex format is selected, the hex character is not uniquely defined. The 1602A will perform all its functions when E1 is displayed. However, the 1602A display cannot provide an unambiguous readout of the trigger word when TRIGGER= is pressed.

E2: Displayed in decimal mode when the stored trigger word contains a mixture of defined and "don't care" states. In decimal, all states in the trigger word must be defined or all must be "don't care." As with E1, the 1602A will perform all its functions when this message is displayed but cannot display the trigger word.

E6: Indicates that operator has attempted to enter an unacceptable character in a trigger word. For example, entering F in octal format or 3 in binary format will generate E6.

E7: Indicates that operator has attempted to enter a trigger word wider than the selected word width.

E13: Indicates that operator has attempted to enter a word width greater than the maximum 16 bits allowed.

E14: Indicates that the operator has tried to enter an alpha character in the word width specification. Word width is a decimal field with only numerals 0-9 as valid entries.

E15: Displayed in mixed format mode to indicate that the operator has attempted to enter a coded word width greater than the specified word width.

E24: Indicates that the operator has tried to select a word number greater than 63 (63 is highest location in 1602A memory).

E25: Indicates that operator has attempted to enter an alpha character in the word number specification. Only numerals 0-9 are allowed in the decimal word number specification.

E30: Indicates that trigger word is not recorded in data memory because start of the data trace was delayed from the trigger word or end of the data trace was delayed more than 63 from the trigger word.

E31: Indicates trigger word did not occur during the last trace cycle. This condition can occur when a trace is terminated with the STOP key.

E40: Indicates that no trigger has occurred for more than three-tenths of a second, but clock and qualifier signals are present.

E41: Indicates that no qualifier has occurred for more than three-tenths of a second, but clocks are present.

E42: Indicates that no clock has occurred for more than three-tenths of a second.

E43: Indicates that one or more specifications that control data recording (e.g. trigger, delay, etc.) has been changed since the last trace cycle. Pressing any display key allows the old data in memory to be accessed.

E44: Indicates that no trace cycle has been executed since the instrument was turned on.

E50: Indicates that the operator has attempted to enter a delay specification greater than the maximum 65 535 allowed.

E51: Indicates that the operator has attempted to enter an alpha character in the decimal delay specification.

E99: Indicates that the 1602A has failed self-test. Refer to Section VIII of this manual for troubleshooting information.

3-43. OPERATOR'S CHECK.

3-44. SELF-TEST. At turn on, the 1602A executes a complete self-test of all circuits except for the keyboard and probe. All internal circuits are tested for proper operation.

3-45. During self-test execution, verify the following:

a. TRACE light in upper-right corner of display flashes.

b. LOGIC POL LEDs alternate.

c. CLOCK EDGE LEDs alternate.

d. TRIGGER PLUS DELAY LEDs alternate.

3-46. Upon completion of self-test (initial conditions), verify the following:

a. Display indicates all 8's. This shows that all circuits and all LED segments are functioning properly.

b. Positive LOGIC POL LED is on.

c. Positive CLOCK EDGE LED is on.

d. TRIGGER PLUS DELAY Starts Trace LED is on.

e. TRACE light is off.

f. Trigger= don't care. Press TRIGGER= key and verify that display shows all dashes.

g. Delay = zero. Press DELAY = key and verify that display shows a "0."

h. Format: Word Width 16, Binary code. Press WORD WIDTH= key and verify that display shows "16" and "b2."

3-47. If a failure occurs during self-test, the error message E99 will be displayed. If E99 is displayed, refer to Section VIII of this manual. The troubleshooting procedure in Section VIII explains how to cycle through self-test in steps. Display messages indicate where the fault is located.

3-48. KEYBOARD AND PROBE TESTING. The keyboard and probe are not tested during self-test, and although the power supply is not specifically tested, it is essentially checked, since improper voltages will cause a failure to occur somewhere during the test sequence.

3-49. Keyboard Test. The keyboard can be tested by cycling the power off then on with key C depressed. This calls up a section of the resident diagnostics that requires all 35 keys to be pressed in predefined order. The order is from upper left (key 1) to lower right (key 35). See figure 3-3.

NOTE

On 1602A Option 001, the rear-panel TALK ONLY/ADDRESSABLE switch must be set to ADDRESSABLE for the keyboard test to function properly.

3-50. When the key test routine is called, a number 1 appears on the left edge of the display. This is a request to press key 1 (LOGIC POL) after which the number 2 appears. After key 2 is pressed, the remaining numbers 3 through 35 will appear as each of the respective keys is pressed.

If any key fails or is pressed out of turn, the right edge of the display will indicate the number of the key read. A "0" at the display indicates that the key could not be

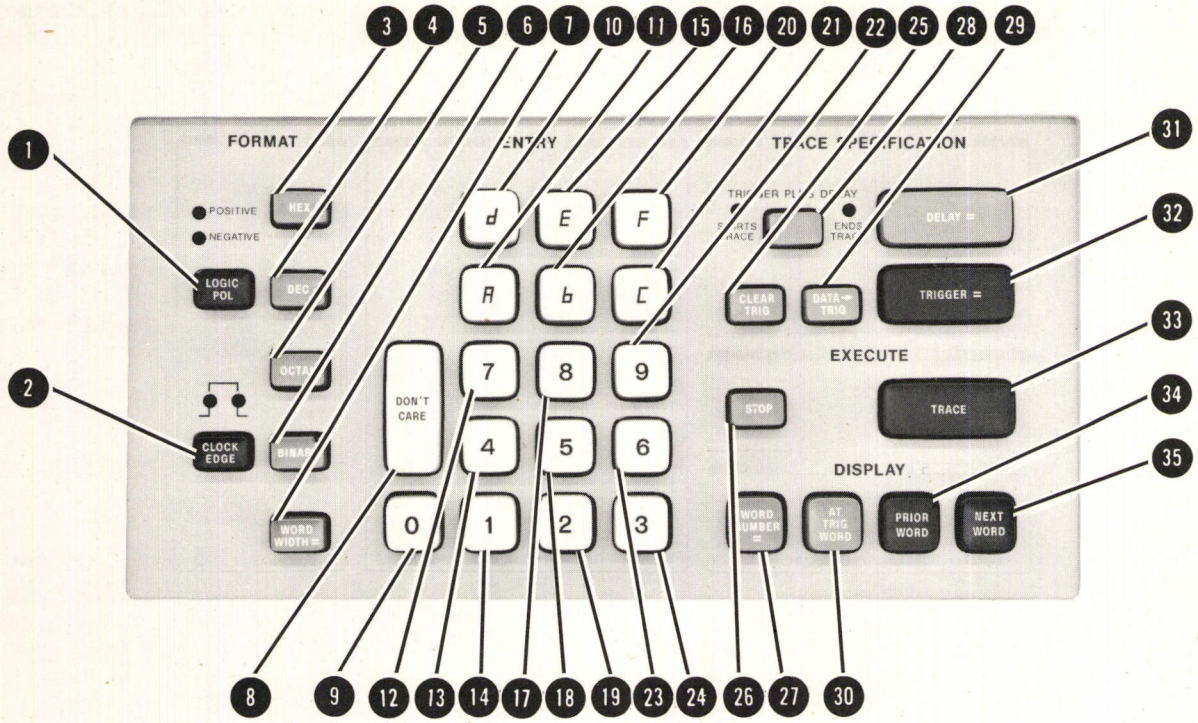


Figure 3-3. Keyboard Test Sequence

recognized and that a hardware failure has occurred. The error message E98 appears, requesting that the key identified at the left side of the display be pressed.

3-51. If within five tries the correct key is not pressed, the instrument will default into the turn-on self-test. The turn-on self-test is also activated upon completion of the keyboard test.

3-52. Probe Test. The probe requires active signals for functional testing. A service probe test source (HP Part No. 5061-1254) is available for exercising the probe. This plug-in accessory is a 16-bit binary counter and derives its power from the probe. Also intended as a service tool, it makes a very effective source for functional testing. To test the probe, select binary code and operate the 1602A in trace continuous mode.

3-53. OPERATING INSTRUCTIONS.

3-54. Operation of the 1602A is very simple with a keyboard that is almost self-explanatory. Simply connect the probe to the system under test, select the desired format using the format keys, define the trace specification, and execute the measurement. The display keys can then be used to view the 64 words stored in memory. Be sure to read "Operating Characteristics" beginning with paragraph 3-5, for a thorough understanding of instrument features before operating the 1602A.

3-55. 1602A OPTION 001 PROGRAMMING.

3-56. Device-dependent commands (ASCII characters) for the 1602A are listed in table 3-1. These commands allow the controller to set the 1602A to desired measurement configurations. The controller can then monitor 1602A measurement results, or they can be sent to other devices (such as a printer).

3-57. In cases where the 1602A is desired to operate in a system without a controller, the 1602A is placed in TALK ONLY mode. This is done with switch A7S1F on 1602A rear panel.

3-58. The 1602A can only respond to its device-dependent commands in remote. In local, it responds to keyboard inputs. In remote, the keyboard inputs are not read (except Return to Local).

3-59. 1602A OPTION 001 DEVICE DEPENDENT COMMAND FORMATTING RULES (HP-IB).

3-60. All device dependent commands are single ASCII uppercase alpha characters. Characters not within the command or data sets are ignored. If data characters (usually numeric) immediately follow a device dependent command that allows data entry, then it is assumed that the string of characters is to modify the selected function, and the data characters are examined by the following rules:

Table 3-1. 1602A Device Dependent Commands

MEASUREMENT DATA FORMAT

B1 ..... sets Hexadecimal
B2 ..... sets Decimal
B3 ..... sets Octal
B4 ..... sets Binary
P1 ..... sets positive logic polarity
P2 ..... sets negative logic polarity
C1 ..... sets positive clock edge
C2 ..... sets negative clock edge
Wx ..... sets word width = x; $2 \leq x \leq 16$*
Fx ..... sets coded subfield width = x; $2 \leq x <$ word width*

*Refer to "Word Width" rules in paragraph 3-12.

TRACE SPECIFICATION

M1 ..... sets Start Trace on Trigger + Delay.
M2 ..... sets End Trace on Trigger + Delay.
Dx ..... sets Delay = x; $0 \leq x \leq 65535_{10}$
Tx ..... sets Trigger = x; x must fit current format exactly.
Ex ..... sets Delay by Trigger Events = x; $0 \leq x \leq 65535_{10}$

EXECUTE

R ..... causes Trace execution and configures 1602A to transmit unformatted data as in U. Aborts any previous Trace in progress.
Z ..... causes Trace Trigger Events (TRACE E) execution and configures 1602A to transmit unformatted data as in U. Aborts any previous Trace in progress.
H ..... halts any Trace in progress.

OUTPUT

Nx ..... configures 1602A to transmit formatted data in memory Word Number = x; $0 \leq x \leq 63_{10}$ (at conclusion of Trace).
U ..... configures 1602A to transmit unformatted data from data memory at conclusion of any Trace in progress
S ..... configures 1602A to transmit Status Byte (8 bits).
L ..... configures 1602A to transmit "Learn" message that defines its measurement configuration.
V ..... Verify; causes 1602A to execute self-test and power-on initialize (except HP-IB status); configures 1602A to transmit self-test result (0 = passed, 16_{10} = failed).

OTHER

I ..... Initialize; causes 1602A to go to power-on configuration (except HP-IB status).

NOTE

All device dependent commands are single ASCII uppercase alpha characters. Characters not within command or data sets are ignored.

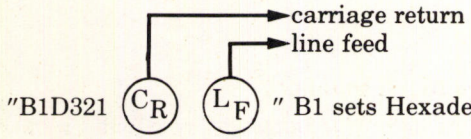
a. Data strings are delimited by any character that could not logically be part of the data message. For example: ";", ".", or "R" each could delimit a data field.

b. Spaces (20 HEX) are ignored except in trigger specifications. ("T")

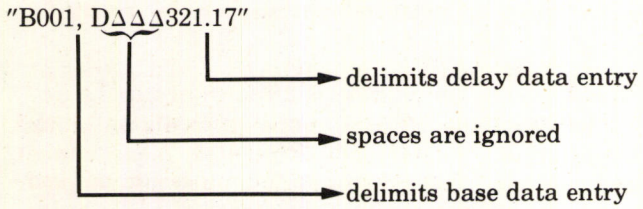
c. Each data string is accepted or rejected as a single quantity when the delimiting character is received. A message appears in the 1602A display when a data string is rejected (E9 for trigger fields, E59 otherwise). The local error indication is intended as a debugging aid to detect out-of-range data, but is removed by the next device dependent command.

d. After the data field has been processed, the delimiting character is processed as a possible device dependent command.

Example: The two device dependent messages described below have the same effect on a 1602A Opt. 001.



trigger word and recorded data. D delimits the base data entry and selects Delay specification. The value 321_{10} is entered as the delay specification. The carriage return delimits the delay data entry.



NOTE

Δ used to indicate a space; ASCII characters are within quote marks (").

3-61. Format Rules for Tx (Trigger Specification).

3-62. Trigger specification (data following "T") has special rules because the 1602A uses "don't Care" ("X") positions in trigger words. Trigger data fields, therefore, are required to follow more restrictive rules to avoid confusion.

a. The trigger word must contain exactly the number and range of data characters needed to uniquely specify a trigger word of the current word width and number base. For example, if word width = 13 and the base is octal, then the specification must contain 5 data characters and only numerics 0 thru 7 and "X" may be used.

b. If the number base is HEX, then ASCII uppercase characters "A," "B," "C," "D," "E," and "F," are added to the numerics and "X" to form the valid data set following a "T." As data characters, these alpha characters do not delimit a HEX trigger field. Therefore, if you wish to follow your HEX trigger word with one of these characters as a device dependent command, use a character in between to delimit the trigger field.

Example: The device dependent message "W16B1T00-B0,D312" requires the comma to delimit the Trigger data entry field. If the comma were removed, the 1602A Opt. 001 would interpret the D as part of Trigger data entry and the Trigger data entry would be rejected because it contains too many characters.

c. If the number base is BINARY, then only "0," "1," or "X" (don't care) are recognized as data characters.

d. If a data character outside the data set is encountered, then the Trigger entry is aborted and the 1602A flashes E9.

e. Leading spaces are ignored.

f. A single space properly positioned after the first data character is used to indicate the boundary between the parts of a split trigger specification. Space(s) in other position(s) cause the specification to be rejected.

3-63. 1602A OUTPUT FORMATS.

3-64. R, Z, or U Commands:

a. Output begins at current memory word number and stops at last word recorded in most recent Trace.

b. Data is transmitted in binary, two bytes per 1602A memory data word, most significant 8 bits first.

c. A maximum of 128 bytes are transmitted.

d. No delimiters or spaces are transmitted.

e. Unspecified bits (in word width) are transmitted as "0." For example; if word width = 10 and 1602A memory word = 1111111111, then 8 MSBs transmitted are 00000011 and 8 LSBs are 11111111.

3-65. Nx Command:

a. Output is data in 1602A memory word number x. The x entry is optional if present word number is the desired word.

b. Data is transmitted at conclusion of Trace if in progress.

c. Word is not repeated until N is again sent to 1602A.

d. Data transmitted in current measurement format (Hex, Binary, etc.).

e. Always 18 characters transmitted; 16 data characters from 1602A memory (right justified), plus carriage return (CR) and line feed (LF).

f. Leading spaces are used to fill 18-character field.

g. If memory word requested was not written into during the last Trace, then 1602A transmits right justified "X"s in current format.

3-66. S Command:

a. When the 1602A receives an "S" it configures to generate a byte that describes its measurement status. The 1602A transmits this status byte when it is addressed to talk and all addressed listeners are ready. The 1602A updates its status byte only when it receives an S or transmits a status byte. The 1602A continues to transmit status bytes until it receives another command. The maximum 1602A status byte transmission rate is approximately 50 bytes/second.

b. Status byte: one 8-bit byte with no delimiters.

bit 0: 1 means 1602A data memory full
bit 1: 1 means Trigger + Delay condition found during last Trace
bit 2: 1 means clock is present
bit 3: 1 means clock qualifier is present
bit 4: 1 means Trace is in progress
bit 5-7: always 0

For example: If 1602A outputs a status of 28 (28_{10}=00011100_2) then a Trace is in progress, clock qualifier and clock are present, Trigger + Delay condition has not been found, and 1602A data memory is not filled.

3-67. V Command:

a. Causes 1602A to execute self-test. See Section VIII of Model 1602A Operating and Service Manual for a description of self-test.

b. Causes 1602A to initialize to power on configuration (except HP-IB status). This power on configuration is the same as sending the 1602A an "I" command. See table 3-1.

Base = BINARY
Clock Slope = POSITIVE
Logic Polarity = POSITIVE
Word Width = 16
Trigger = DON'T CARE
Delay = 0
Trigger + Delay = STARTS TRACE
Display = all 8s

c. Causes 1602A to transmit self-test result. 1602A transmits 0 for passed and 16_{10} for failed. When 1602A sends 0 to indicate self-test passed, there still exists a possibility that the 1602A is not completely functional. The operator should check the 1602A display and front-panel indicators to verify that it has initialized as shown above.

NOTE

Either the I or Vcommand is used to Clear the 1602A. The 1602A will not respond to other clear messages on the HP-IB.

3-68. L Command:

3-69. If a 1602A measurement needs to be duplicated at some future time, then the 1602A may be placed in the "learn" mode. This causes the 1602A to transmit a message that defines its measurement configuration. If this message is stored and later transmitted to the 1602A, then the measurement is automatically repeated.

3-70. "Learn" mode procedure:

a. Send "L" to 1602A.

b. Address 1602A to talk.

c. Read 12 byte (8 bits/byte) message from 1602A.

d. Save this returned message.

3-71. When the measurement needs to be repeated:

a. Address 1602A to listen.

b. Send the 12 byte message to 1602A. 1602A reconfigures, automatically executes measurement, and prepares to return binary data upon measurement conclusion.

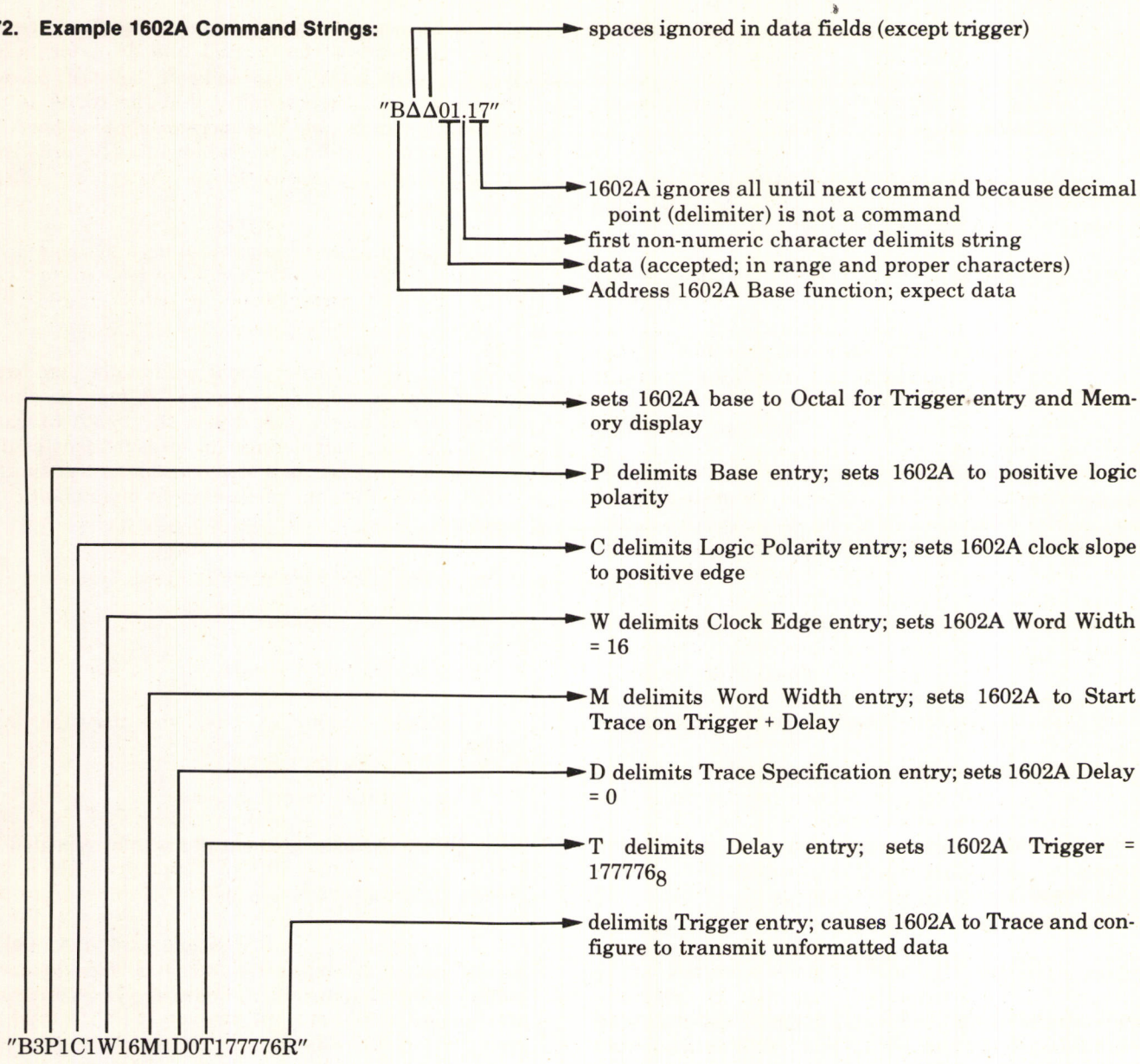
c. Address 1602A to talk.

d. Read measurement result from 1602A.

NOTE

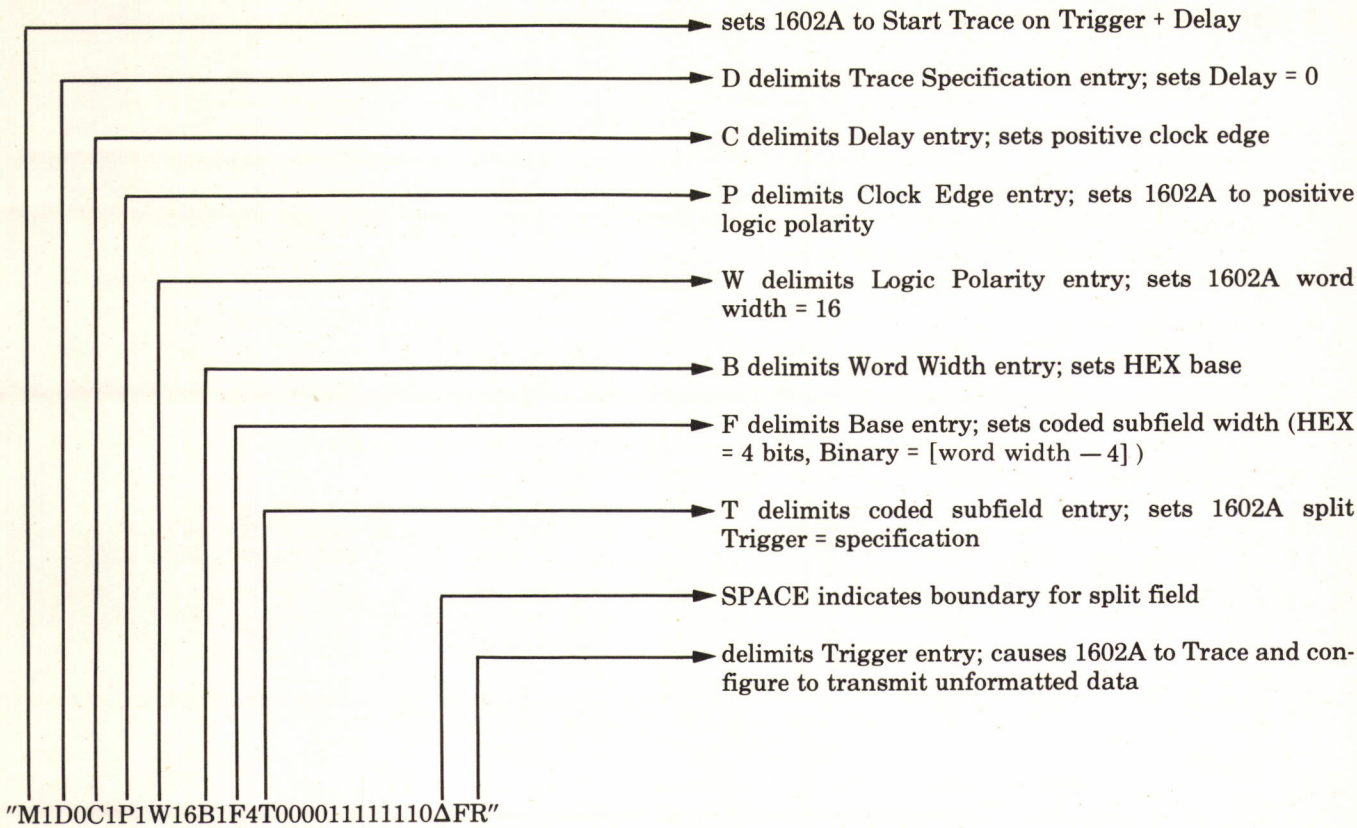
The first byte of the 12 byte message sent by 1602A is an ASCII "J." When the 1602A receives an ASCII "J," the next 11 bytes are loaded into its internal registers without qualification. It is recommended that "J" be used only in messages generated by a 1602A in response to an "L," as minor changes in message content can cause nonrecoverable states in the 1602A. If the 1602A has been put in a nonrecoverable state, it will not respond properly to front-panel controls. The line power switch must be cycled off and on, and any measurements that were in process must be restarted.

3-72. Example 1602A Command Strings:



Upon Trace completion:

If 1602A is addressed to talk, the first two bytes transmitted will be 255 254 (assuming 1602A memory word number = 0). These indicate that 1602A memory word 0 contains 11111111_2 (= 255_{10}) in 8 MSBs and 11111110_2 (= 254_{10}) in 8 LSBs. This equals 177776_8 (Trigger word).



Upon Trace completion:

If the 1602A is sent the message "N 0;" (with delimiter after 0, such as ";") and addressed to talk, it will return ΔΔ 000011111110ΔF to the controller. This is the content of 1602A memory line 0 expressed in 1602A current format.

3-73. TRACE/RETURN TO LOCAL KEY.

3-74. In local, the 1602A will respond to front panel keys only. When the 1602A is in "remote," all front panel keys are ignored except RETURN TO LOCAL key, and REMOTE light (lower right corner of display) is on. The 1602A is put in remote operation when it receives its listen address and REN is low. Local operation is obtained when: (a) 1602A RETURN TO LOCAL key is pressed, or (b) HP-IB controller puts REN line high, or (c) controller sends "Go to Local" message.

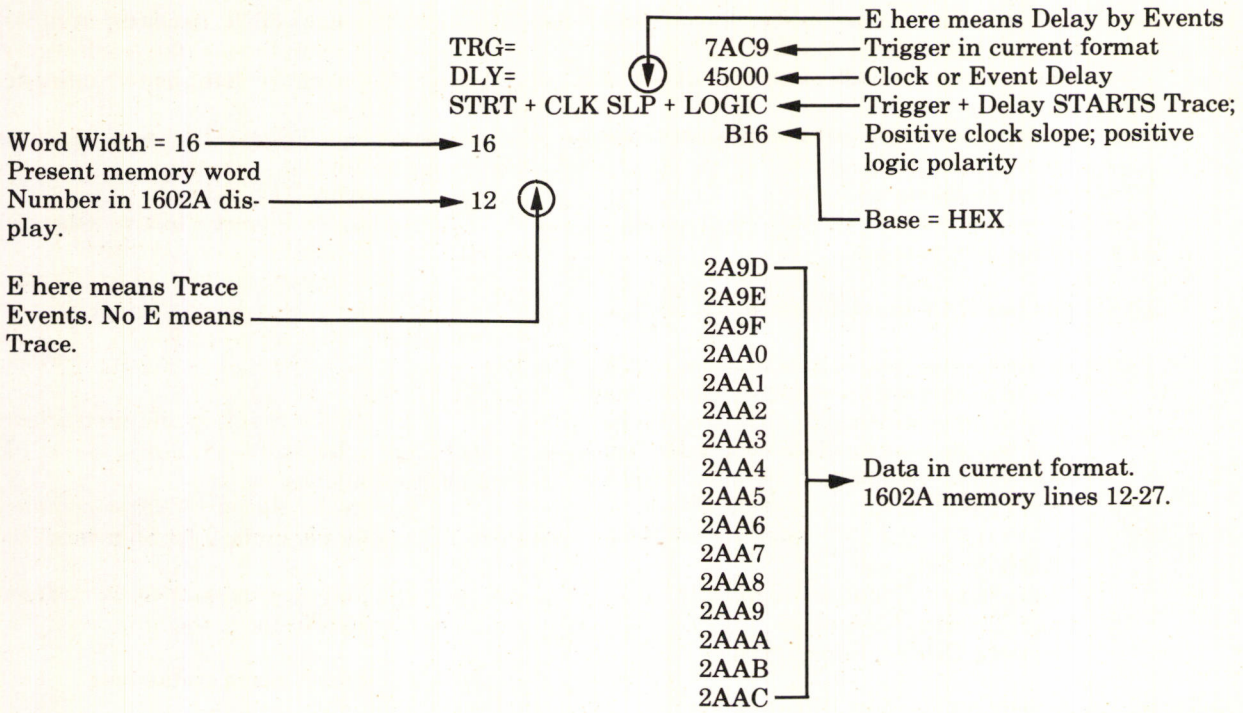
3-75. STOP/PRINT KEY.

3-76. If a Trace is in progress, the STOP key functions normally. If no Trace is in progress, the STOP/PRINT key performs PRINT function. PRINT key causes 1602A to configure to send a message to the listener(s) via HP-IB.

3-77. This message shows current 1602A measurement configuration and 16 lines of 1602A memory starting with present word number. If the 16 lines go past memory line 63, then all message lines after the one for line 63 are shown as Xs. 1602A memory locations that were not written into during the last Trace are also shown as Xs in appropriate lines of the 16 line message.

3-78. The message data output from 1602A is formatted to fit a 20 column printer (for example, an HP Model 5150A Opt 001 Thermal Printer).

Example:



3-79. The 1602A display memory is shared as a buffer for HP-IB input and output operations. Therefore, the content of the 1602A display following HP-IB communication is not significant.

3-80. 1602A Opt 001 (HP-IB) CHECKOUT PROGRAMS.

3-81. HP Model 9830A Checkout Program.

3-82. The program below is written for an HP 9830A controller. The extended I/O ROM (11272 or Opt 272) must be installed in the 9830A before the program can be executed. The program can be run without a data source for the 1602A, or with the 16-bit Probe Test Source (HP Part No. 5061-1254) connected to 1602A Data Probe A5.

```
 10 FORMAT B
 20 OUTPUT (13,10) 768;
 30 CMD "?U/ ","V ","?O5"
 40 V=RBYTE13
 50 PRINT V
 60 STOP
 70 CMD "?U/ ","B1P2C2M2D0W16T0000R"
 80 WAIT 300
 90 CMD "?U/ ","S ","?05"
100 S=RBYTE13
110 PRINT S
120 OUTPUT (13,10) 1024;
130 END
```

Explanation:

LINE 10: sets format for output statements

20: sets bus REN line LO (true)

30: commands 1602A to perform internal verification and transmit result.

40: 9830A (controller) reads the verification result (output by 1602A)

50: 9830A prints byte

60: stop program - verification byte (V) from 1602A should be checked for a value of 0 (passed) or 16_{10} (failed). This indicates 1602A self-test result. Verify that 1602A front-panel indications are as follows:
Display = all 8s
REMOTE light on
Clock Slope = Positive edge
Logic Polarity = Positive
Trigger + Delay = Starts Trace

To continue program, press 9830A

CONT	(continue)

EXECUTE	Keys

70: 1602A is set up and instructed to execute a Trace.

80: delay allows 1602A to complete Trace if 16-bit Probe Test Source (5061-1254) is used

90: 1602A commanded to transmit status bytes

100: 9830A reads status byte

110: status byte printed

120: sets bus REN line HI (false)

130: ends program - status byte (S) from 1602A should be checked for a value of 15 (decimal equivalent of status byte with 16-bit Probe Test Source connected) or 16 (Probe Test Source not connected). Verify 1602A front-panel indications as follows:

REMOTE light off
Clock Slope = Negative Edge
Logic Polarity = Negative
Trigger + Delay = Ends Trace

3-83. HP Model 9825A Checkout Program.

3-84. The program below is written for an HP 9825A controller. The program can be run without a data source for the 1602A, or with the 16-bit Probe Test Source (HP Part No. 5061-1254) connected to 1602A Data Probe A5. Set 9825A I/O card to "7".

```
 0: rem 7
 1: wrt 715, "V"
 2: rdb (715)→V
 3: prt V
 4: stp
 5: wrt 715, "B1P2C2M2D0W16T0000R"
 6: wait 300
 7: wrt 715, "S"
 8: rdb (715)→S
 9: prt S
10: lcl 7
11: end
```

Explanation:

LINE 0: sets bus REN line LO (true)

1: commands 1602A to perform internal verification

2: 9825A reads verification byte

3: 9825A prints verification byte

4: stop program — verification byte (V) from 1602A should be checked for a value of 0 (passed) or 16_{10} (failed). This indicates 1602A self-test result. Verify 1602A front-panel indications as follows:

Display = all 8s
REMOTE light on
Clock Slope = Positive Edge
Logic Polarity = Positive
Trigger + Delay = Starts Trace

To continue program, press 9825A key CONTINUE

5: 1602A is set up and instructed to execute a trace

6: delay allows 1602A to complete Trace if 16-bit Probe Test Source is used

7: 1602A commanded to transmit status bytes

8: 9825A reads status byte

9: 9825A prints status byte

10: sets bus REN line HI (false)

11: ends program — status byte (S) from 1602A should be checked for a value of 15 (decimal equivalent of status byte with 16-bit Probe Test Source connected) or 16 (Probe Test Source not connected). Verify 1602A front-panel indications as follows:

REMOTE light off
Clock Slope = Negative Edge
Logic Polarity = Negative
Trigger + Delay = Ends Trace

3-85. INSTRUMENT CLEANING.

3-86. Clean the 1602A with a soft cloth dampened in water containing a mild detergent.

CAUTION

Never use industrial solvents or abrasive cleaners which can damage the display window and instrument surfaces. Do not allow liquid to penetrate through the keyboard and into the 1602A.

SECTION IV

PERFORMANCE TESTS

4-1. INTRODUCTION.

4-2. The procedures in this section test Model 1602A electrical performance using specifications in table 1-1 as the performance standard. All tests can be performed without access to the interior of the instrument.

4-3. EQUIPMENT REQUIRED.

4-4. Equipment required for the performance tests is listed in the Recommended Test Equipment table in Section I. Any equipment that satisfies critical specifications given in the table may be substituted for the recommended models.

4-5. TEST RECORD.

4-6. Results of the performance tests may be tabulated on the Performance Test Record at the end of the procedures. The Test Record lists all tested specifications and their acceptable limits. The results recorded at incoming inspection can be used for comparison in periodic maintenance and troubleshooting and after repairs.

4-7. OPERATION VERIFICATION.

4-8. The following procedure is an abbreviated test that provides approximately 90% assurance of proper 1602A operation. Table 1-1 specifications are not tested in the abbreviated test.

a. Perform Operator's Check (Self-Test and Keyboard Test) in Section III.

b. Connect Probe Test Source (HP Part No. 5061-1254) to 1602A probe pod and set 1602A Format and Trace specifications as follows:

FORMAT
Logic Polarity ..... Negative
Clock Edge ..... ⌐
Word Width= 16
Base ..... Hex

TRACE SPECIFICATION
Trigger Plus Delay ..... Ends Trace
Delay= 63
Trigger ..... FFFF

c. Press TRACE key. Verify that display shows:

FFFF in memory word 0 and FFFE in memory word 1.

0	FFFF	FFFE

4-9. TEST SIGNAL CONNECTIONS.

4-10. No standard adapter is available for connecting test signals to the 1602A probe. It is therefore recommended that short lengths of solid wire be inserted in BNC-to-alligator clip adapters; 1602A probe grabbers can then be connected to the wires.

PERFORMANCE TESTS

4-11. CLOCK, DATA, AND CLOCK QUALIFIER PROBE INPUTS TESTS.

SPECIFICATIONS:

REPETITION RATE: 10-Mhz maximum.

MINIMUM INPUT SWING: from ≤+0.4 V (LOW) to ≥+2.4 V (HIGH).

CLOCK PULSE WIDTH: ≥25 ns at threshold.

SETUP TIME: (time data must be present at 1602A probe input before clock transition) 35 ns at threshold.

HOLD TIME: (time data must be present at 1602A probe input after clock transition) 0 ns.

DESCRIPTION:
Pulses are applied to 1602A Probe inputs. Pulse periods, widths, delays, and amplitudes are varied. In each case, the resulting 1602A display is checked to verify proper operation for the specification being tested.

PERFORMANCE TESTS

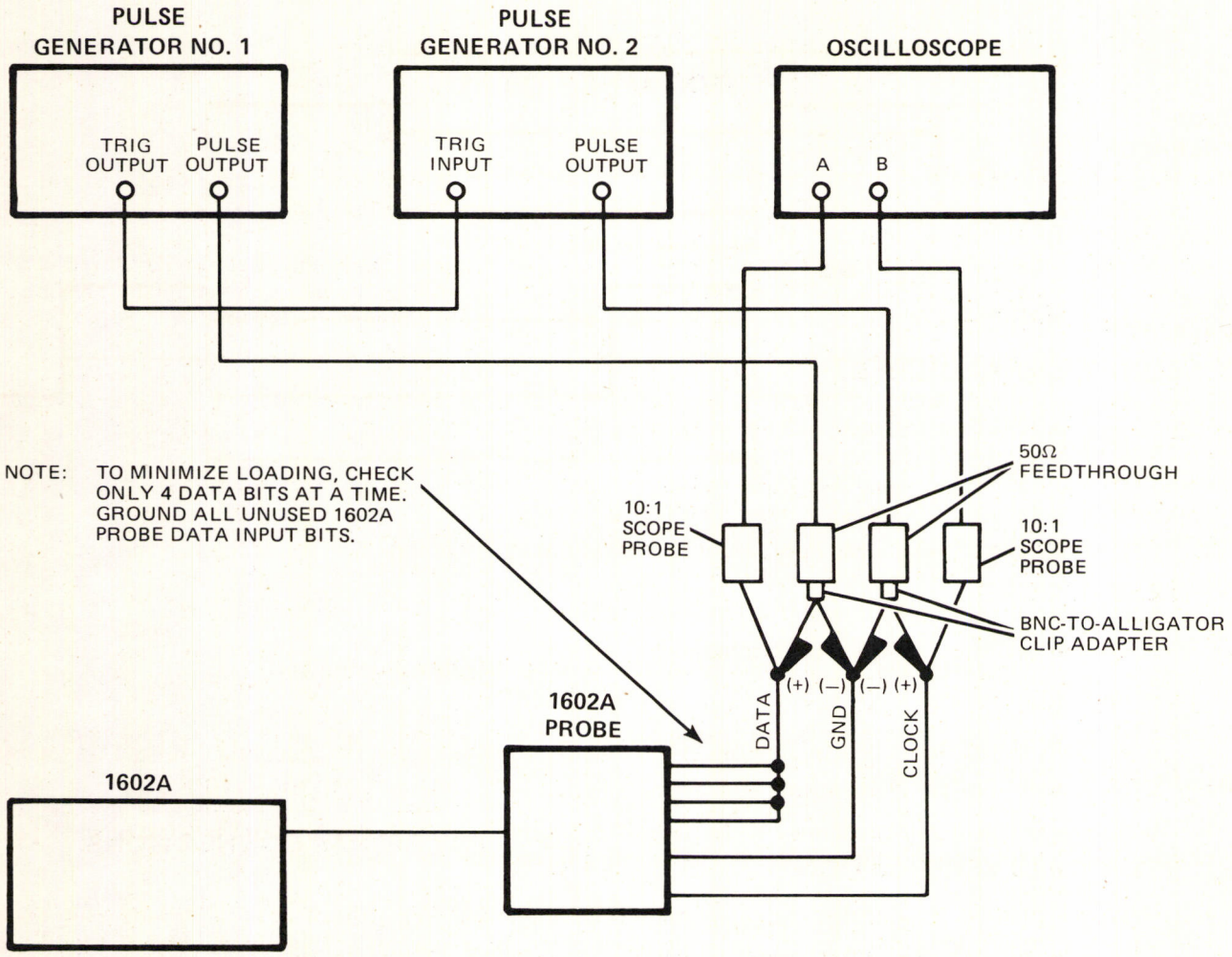


Figure 4-1. Clock, Data, and Clock Qualifier Probe Inputs Test Setup

EQUIPMENT:

Pulse Generators (2)	HP 8012B
Dual-Channel Oscilloscope	HP 1740A
Feedthrough Terminations (2)	HP 10100C
BNC-to-Alligator Clip Adapters(s)	HP Part No. 8120-1292

PROCEDURE:

a. Connect test equipment as shown in figure 4-1.

NOTE

To minimize loading, check only four 1602A Probe input data bits at a time. Ground all unused data bit inputs.

b. Adjust pulse generator outputs as shown in figure 4-2.

c. Set 1602A Format and Trace Specifications as follows:

Format: Logic Polarity = Positive
Clock Edge = ⌐¬
Word Width = 16
Base = Binary

PERFORMANCE TESTS

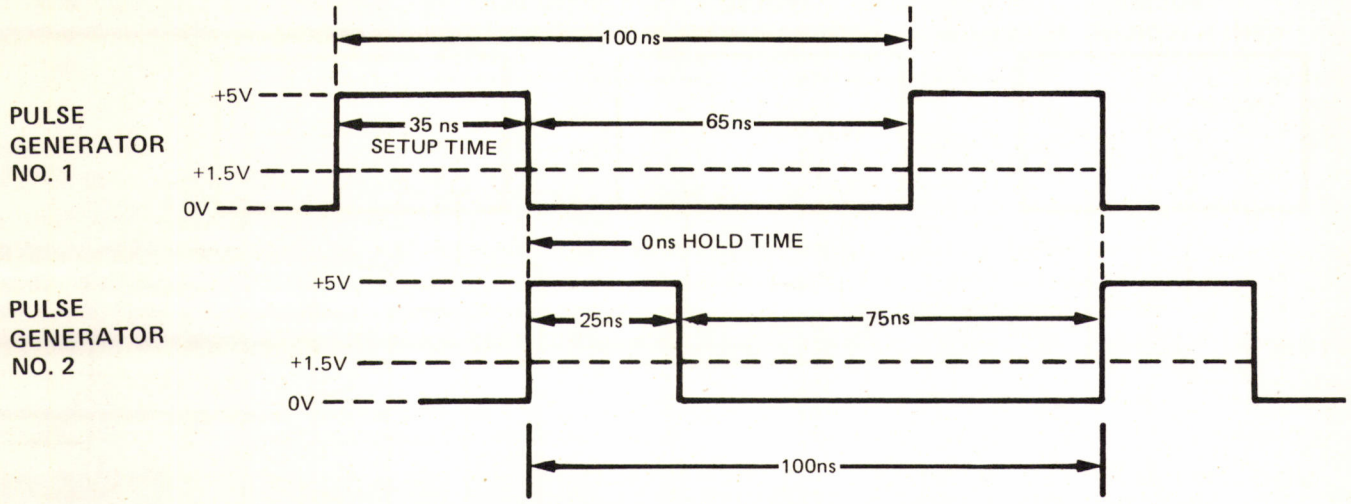


Figure 4-2. Clock, Data, and Clock Qualifier Probe Inputs Test Waveforms

Trace Specification: Trigger + Delay = Starts Trace
Delay = 0
Trigger = 1111 for data bits being tested; 0 for all other data inputs.

d. Press TRACE key, then C key (places 1602A in Trace Continuous mode). 1602A should display 1111 for data inputs (bits) connected to test signal.

e. Vary pulse period of pulse generator No. 1 (figure 4-2). Verify that 1111 is displayed for bits tested when pulse periods are ≥100 ns (repetition rate ≤10 MHz). This verifies repetition rate specification.

f. Vary clock pulse width and delay (pulse generator No. 2, figure 4-2). Verify that 1111 is displayed for bits tested with 35 ns setup time, 0 hold time, and 25 ns wide clock pulse. A display of 1111 verifies setup and hold time specifications for data bits tested, and clock width specification.

g. Adjust pulse generators No. 1 and No. 2 as shown in figure 4-3. Verify that 1111 is displayed for data bits tested when input from pulse generator No. 1 is ≥+2.4 V.

h. Set 1602A Trigger = "don't care" (all dashes on display). Press TRACE key, then C key. Adjust pulse generators No. 1 and No. 2 as shown in figure 4-4. Verify that 1602A display shows all zeros when input from pulse generator No. 1 is ≤+0.4 V. Correct display for steps g and h verify minimum input swing specification.

i. Repeat steps a through h for the remaining 12 Probe input data bits.

j. Remove all connections from Probe input data bits.

k. Connect pulse generator No. 1 to 1602A Probe CLOCK QUAL input.

NOTE

Probe Wire-Adapter Assembly A6 does not have a wire for Probe A5 Clock Qual input. It is recommended that A6 covers be removed and the pulse generator output be held on Probe A5 Clock Qual input by the person performing the test.

l. Adjust pulse generator outputs for waveforms as shown in figure 4-2.

m. Set 1602A Trigger = "don't care." Press TRACE key, then C key.

PERFORMANCE TESTS

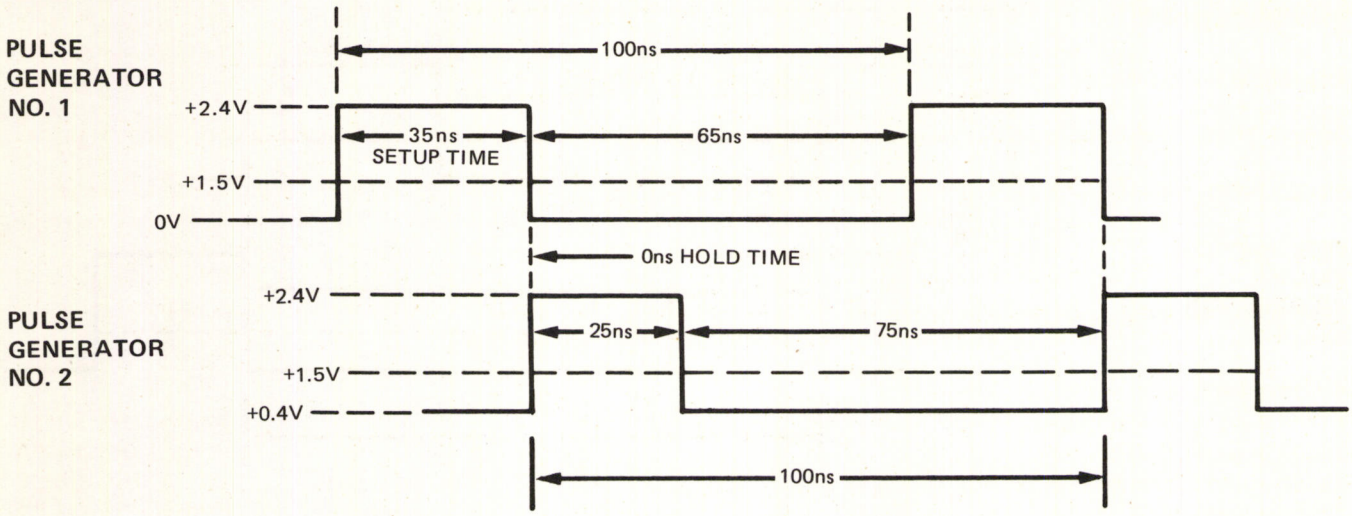


Figure 4-3. Probe Minimum Swing (Minimum High) Test Waveforms

n. Vary pulse generator No. 2 pulse position (figure 4-2) until no qualifier condition is observed (1602A displays message E41). Verify that qualifier conditions are valid (data displayed by 1602A) for 35 ns setup time and 0 ns hold time.

o. Adjust pulse generators No. 1 and No. 2 as shown in figure 4-3. Verify that qualifier condition is valid when input from pulse generator No. 1 is $\geq$+2.4 V.

p. Adjust pulse generators No. 1 and No. 2 as shown in figure 4-4. Verify that qualifier condition is invalid (message E41 displayed) when input from pulse generator No. 1 is $\leq$+0.4 V. Steps o and p verify minimum input swing specification.

q. Replace Wire-Adapter Assembly covers if removed.

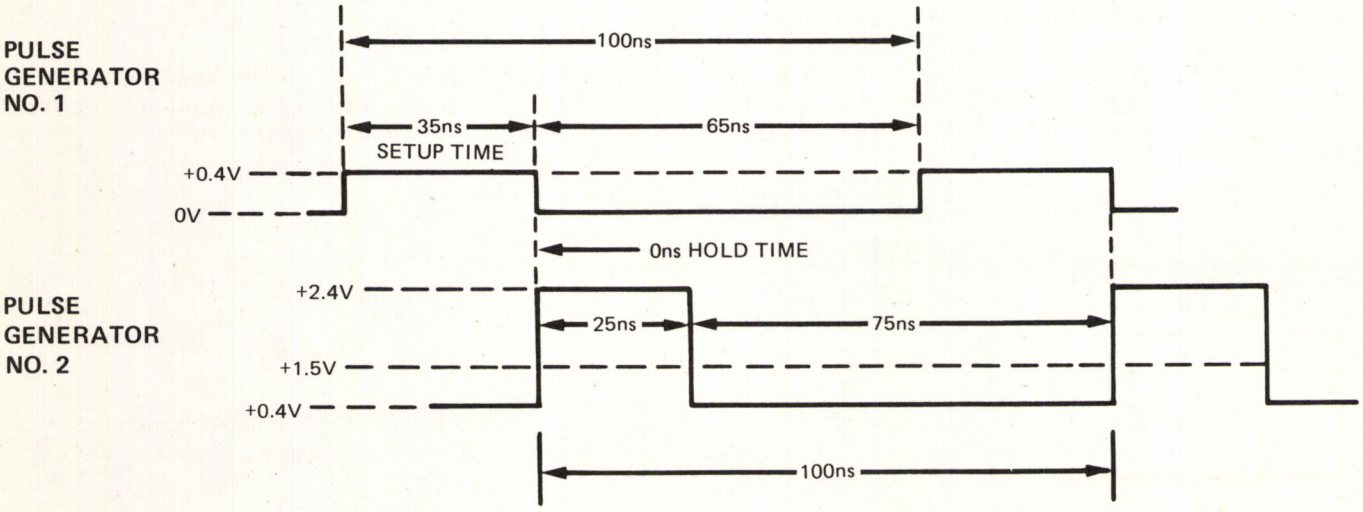


Figure 4-4. Probe Minimum Swing (Maximum Low) Test Waveforms

PERFORMANCE TESTS

4-12. TRIGGER QUALIFIER AND CLOCK QUALIFIER INPUTS (REAR PANEL) TESTS.

SPECIFICATIONS:

MINIMUM INPUT SWING: from $\leq +0.4$ V (LOW) to $\geq +2.5$ V (HIGH).

SETUP TIME: time data must be present before clock transition, 40 ns with Model 10250A probe, 10 ns without probe.

HOLD TIME: time data must be present after a clock transition, 15 ns with 10250A probe, 30 ns without probe.

DESCRIPTION:
Pulses are applied to 1602A Probe Clock input and to 1602A rear-panel CLOCK QUAL input. Pulse delays and amplitudes are varied. In each case, the resulting 1602A display is checked to verify proper 1602A operation for the specifications being tested. This procedure is repeated for TRIG QUAL input.

EQUIPMENT:

PULSE GENERATORS (2)	HP 8012B
Dual-Channel Oscilloscope	HP 1740A
Feedthrough Termination	HP 10100C
BNC-to-Alligator Clip Adapter	HP Part No. 8120-1292
BNC Tee Connector	HP Part No. 1250-0781
BNC Adapter Tip	HP 10011B

PROCEDURE:

a. Connect test equipment as shown in figure 4-5 with pulse generator No. 1 connected to 1602A rear-panel CLOCK QUAL input.

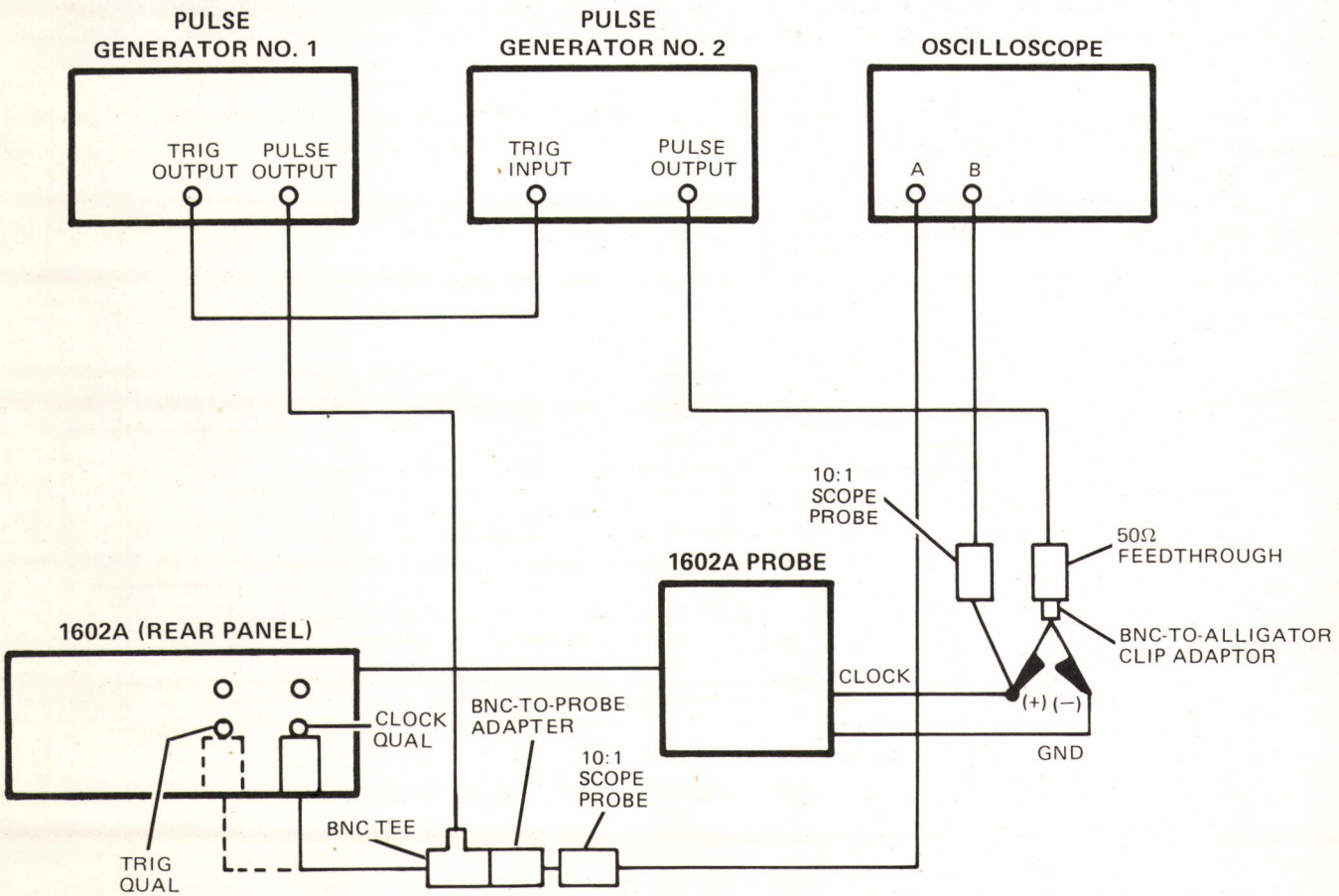


Figure 4-5. Trigger Qualifier and Clock Qualifier Inputs (Rear Panel) Test Setup

PERFORMANCE TESTS

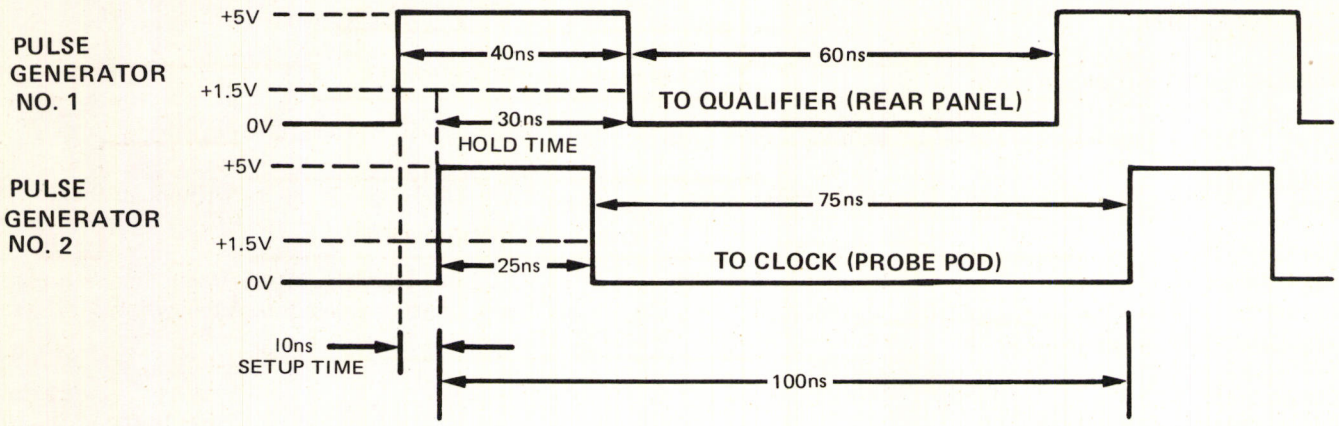


Figure 4-6. Trigger Qualifier and Clock Qualifier Inputs (Rear Panel) Test Waveforms

b. Adjust pulse generator outputs as shown in figure 4-6.

c. Set 1602A Trigger = "don't care" (all dashes in display). Press TRACE key, then C key (places 1602A in Trace Continuous mode).

d. Vary pulse generator No. 2 pulse position (figure 4-6) until no qualifier condition is observed (1602A displays message E41). Verify that qualifier conditions are valid (data displayed by 1602A) for 10 ns setup time and 30 ns hold time.

e. Adjust pulse generators No. 1 and No. 2 as shown in figure 4-7. Verify that qualifier condition is valid when pulse generator No. 1 input is $\geq$+2.4 V.

f. Adjust pulse generators No. 1 and No. 2 as shown in figure 4-8. Verify that qualifier condition is invalid (message E41 displayed) when pulse generator No. 1 input is $\leq$+0.4 V. Steps e and f verify minimum input swing specification.

g. Connect pulse generator No. 1 to 1602A rear-panel TRIG QUAL input and repeat steps b through f.

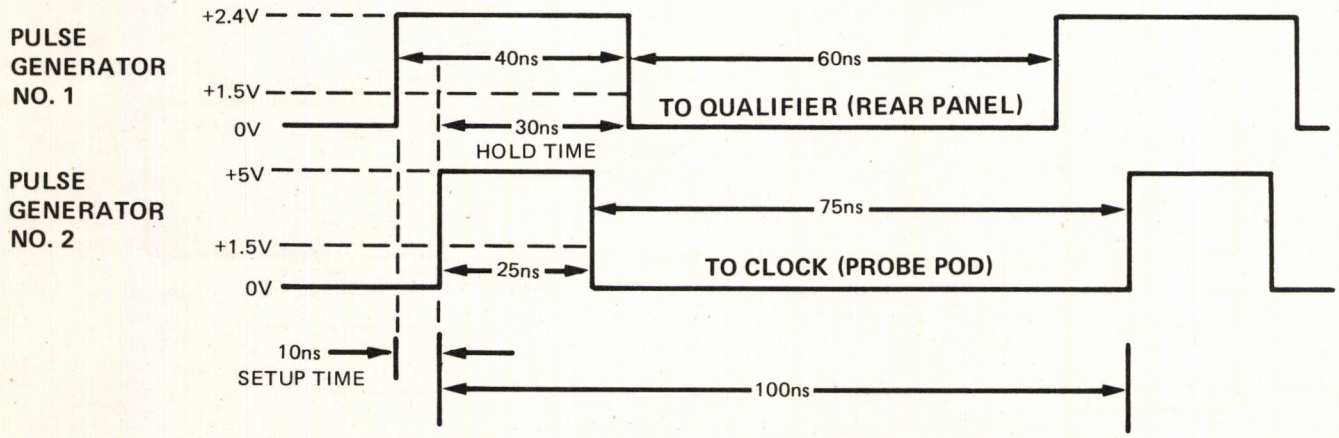


Figure 4-7. Minimum High Inputs (Rear Panel) Test Waveforms

PERFORMANCE TESTS

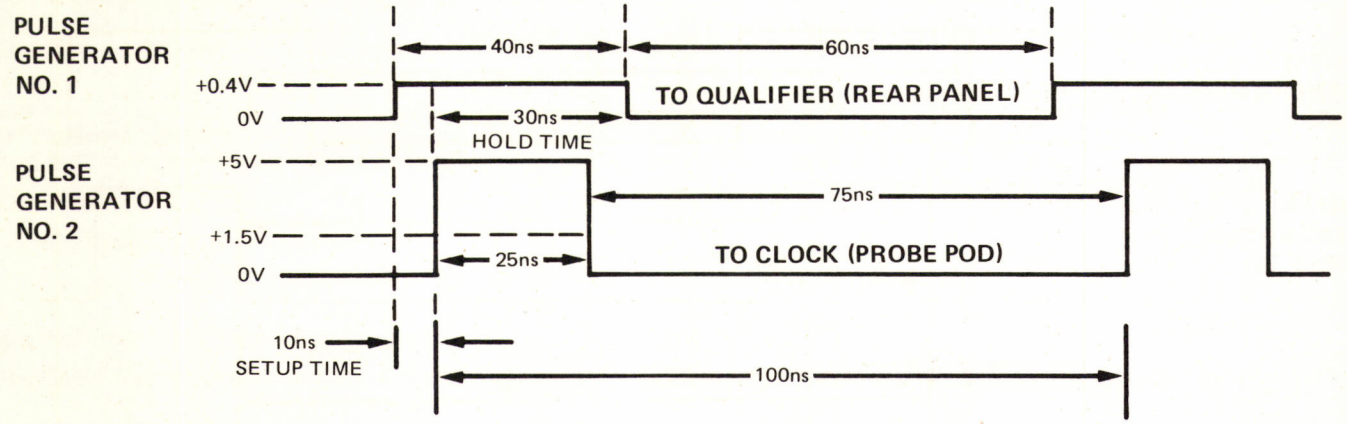


Figure 4-8. Maximum Low Inputs (Rear Panel) Test Waveforms

4-13. TRIGGER AND TRACE POINT OUTPUTS TESTS.

SPECIFICATIONS:

High: ≥2 V into 50Ω.
Low: ≤0.4 V into 50Ω.

DESCRIPTION:

A Probe Test Source (16-bit binary counter) is connected to 1602A Probe. 1602A is placed in Trace Continuous mode to provide repetitive pulses from rear-panel TRIG OUT and TRACE POINT OUT connectors. Amplitudes of these pulses are checked to verify output voltage specifications for high and low states.

EQUIPMENT:

Probe Test Source ..... HP Part No. 5061-1254
Dual-Channel Oscilloscope ..... HP 1740A

PROCEDURE:

a. Connect test equipment as shown in figure 4-9.

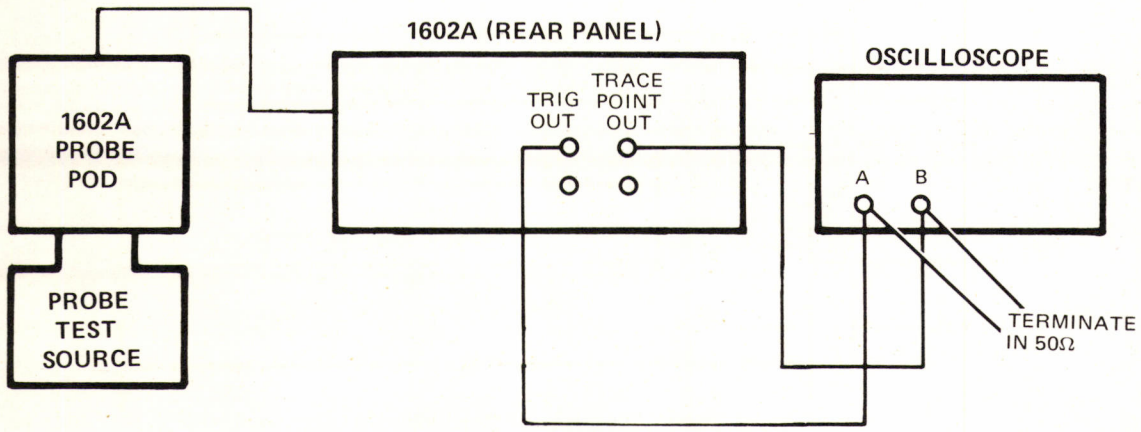


Figure 4-9. Trigger and Trace Point Outputs Test Setup

PERFORMANCE TESTS

b. Connect Probe Test Source (HP Part No. 5061-1254) to 1602A Probe pod.

c. Set 1602A format and trace specification as follows:

Format: Logic Polarity = Positive
Clock Edge = ⌐¬
Word Width = 16
Base = Hex
Trace Specification: Trigger + Delay = Starts Trace
Delay = 1
Trigger = - - - - (dashes indicate "don't cares").

d. Press TRACE key then C key (places 1602A in Trace Continuous mode.)

e. Observe TRACE POINT OUT signal. Verify that pulse amplitude is $\geq$+2 V (into 50 Ω) for logic high and $\leq$+0.4 V (into 50 Ω) for logic low.

f. Observe TRIG OUT signal. Verify that pulse amplitude is $\geq$+2 V (into 50Ω) for logic high and $\leq$+0.4 V (into 50Ω) for logic low.

PERFORMANCE TEST RECORD

HEWLETT-PACKARD

MODEL 1602A

LOGIC STATE ANALYZER

Tested By _____

Serial No. _____ **Date** _____

Paragraph Number	Test	Specification	Passed	Failed
4-11	CLOCK, DATA, AND CLOCK QUALIFIER PROBE INPUTS			
4-11e	Repetition Rate	≤10 MHz		
4-11f	Setup Time (Data)	≥35 ns		
	Hold Time (Data)	≥0 ns		
	Clock Pulse Width	≥25 ns		
4-11g,	Minimum Input (Clock and Data)	≥+2.4 V High ≤+0.4 V Low		
4-11n	Setup Time (Clock Qual)	≥35 ns		
	Hold Time (Clock Qual)	≥0 ns		
4-11o, p	Minimum Input (Clock Qual)	≥+2.4 V High ≤+0.4 V Low		
4-12	TRIGGER QUALIFIER AND CLOCK QUALIFIER INPUTS (REAR PANEL)			
4-12d	Setup Time (Clock Qual)	≥10 ns		
	Hold Time (Clock Qual)	≥30 ns		
4-12e, f	Minimum Input (Clock Qual)	≥+2.4 V High ≤+0.4 V Low		
4-12g	Setup Time (Trig Qual)	≥10 ns		
	Hold Time (Trig Qual)	≥30 ns		
	Minimum Input (Trig Qual)	≥+2.4 V High ≤+0.4 V Low		
4-13	TRIGGER AND TRACE POINT OUTPUTS			
4-13e	Level (Trace Point Out)	≥+2.0 V High ≤+0.4 V Low		
4-13f	Level (Trig Out)	≥+2.0 V High ≤+0.4 V Low		

SECTION V

ADJUSTMENTS

The Model 1602A has no adjustments.

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information for ordering parts. Table 6-1 lists abbreviations used in the parts list and throughout the manual. Table 6-2 lists all replaceable parts in reference designator order. Table 6-3 contains the names and addresses that correspond to the manufacturers' five-digit code numbers.

6-3. ABBREVIATIONS.

6-4. Table 6-1 lists abbreviations used in the parts list, the schematics and throughout the manual. In some cases, two forms of the abbreviation are used: one all in capital letters, and one partial or no capitals. This occurs because the abbreviations in the parts list are always all capitals. However, in the schematics and other parts of the manual, other abbreviation forms are used with both lowercase and uppercase letters.

6-5. REPLACEABLE PARTS LIST.

6-6. Table 6-2 is the list of replaceable parts and is organized as follows:

a. Chassis-mounted parts in alphanumerical order by reference designation.

b. Electrical assemblies and their components in alphanumerical order by reference designation.

c. Option parts.

The information given for each part consists of the following:

a. The Hewlett-Packard part number.

b. The total quantity (Qty) in the instrument.

c. The description of the part.

d. A five-digit code that indicates the manufacturer.

e. The manufacturer's part number.

The total quantity for each part is given only once—at the first appearance of the part number in the list.

6-7. ORDERING INFORMATION.

6-8. To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number, indicate the quantity required, and address the order to the nearest Hewlett-Packard office.

6-9. To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument serial number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard office.

6-10. DIRECT MAIL ORDER SYSTEM.

6-11. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

b. No maximum or minimum on any mail order (there is a minimum order amount, for parts ordered through a local HP office when the orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices—to provide these advantages, a check or money order must accompany each order.

6-12. Mail-order forms and specific ordering information are available through your local HP office. Addresses and phone numbers are located at the back of this manual.

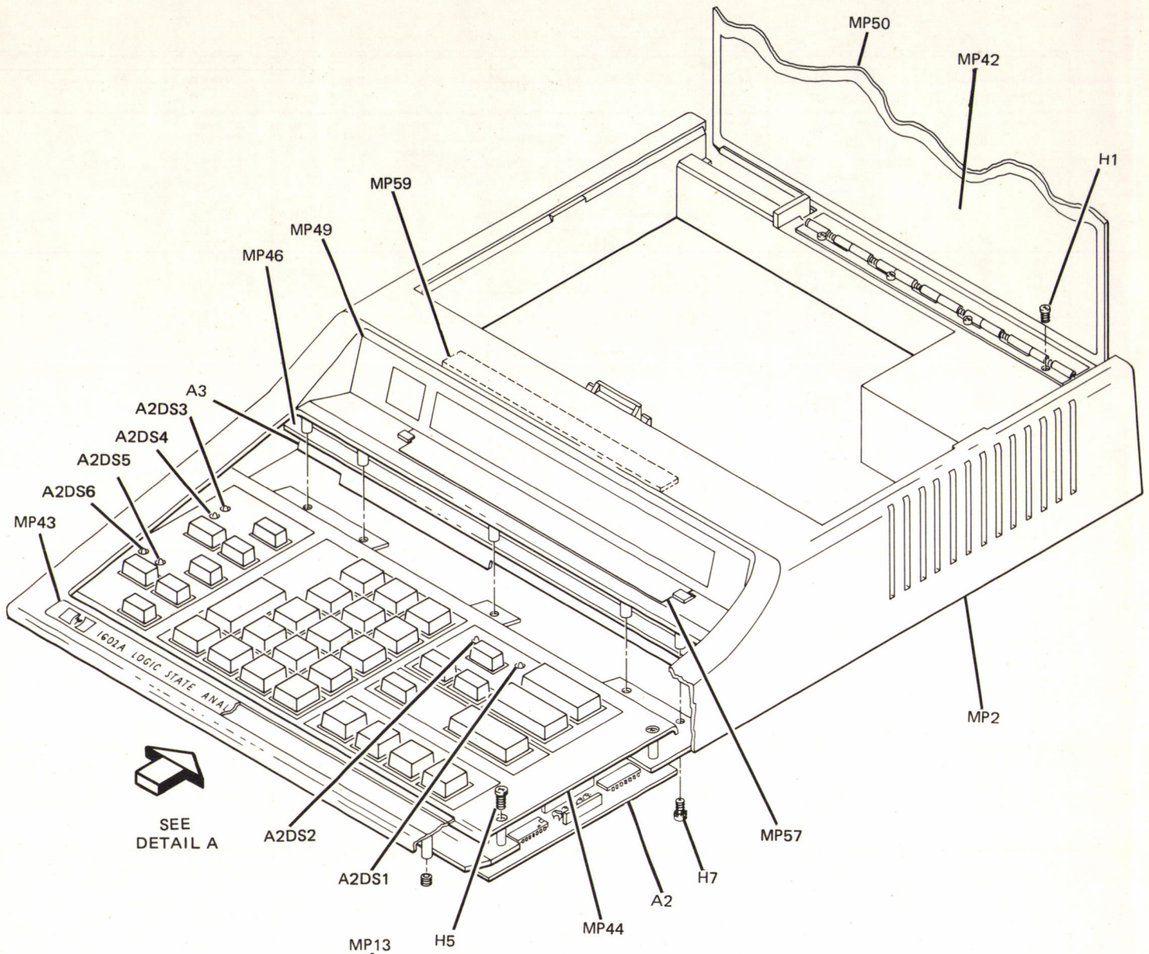
Table 6-1. Reference Designators and Abbreviations

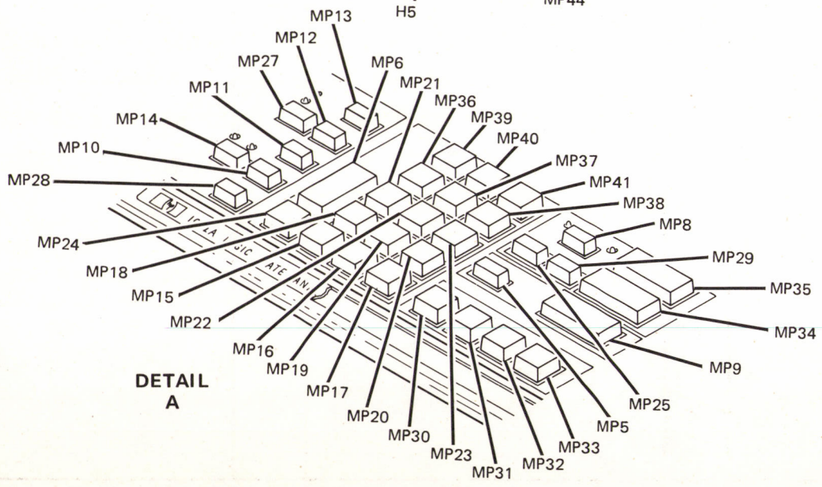
REFERENCE DESIGNATORS

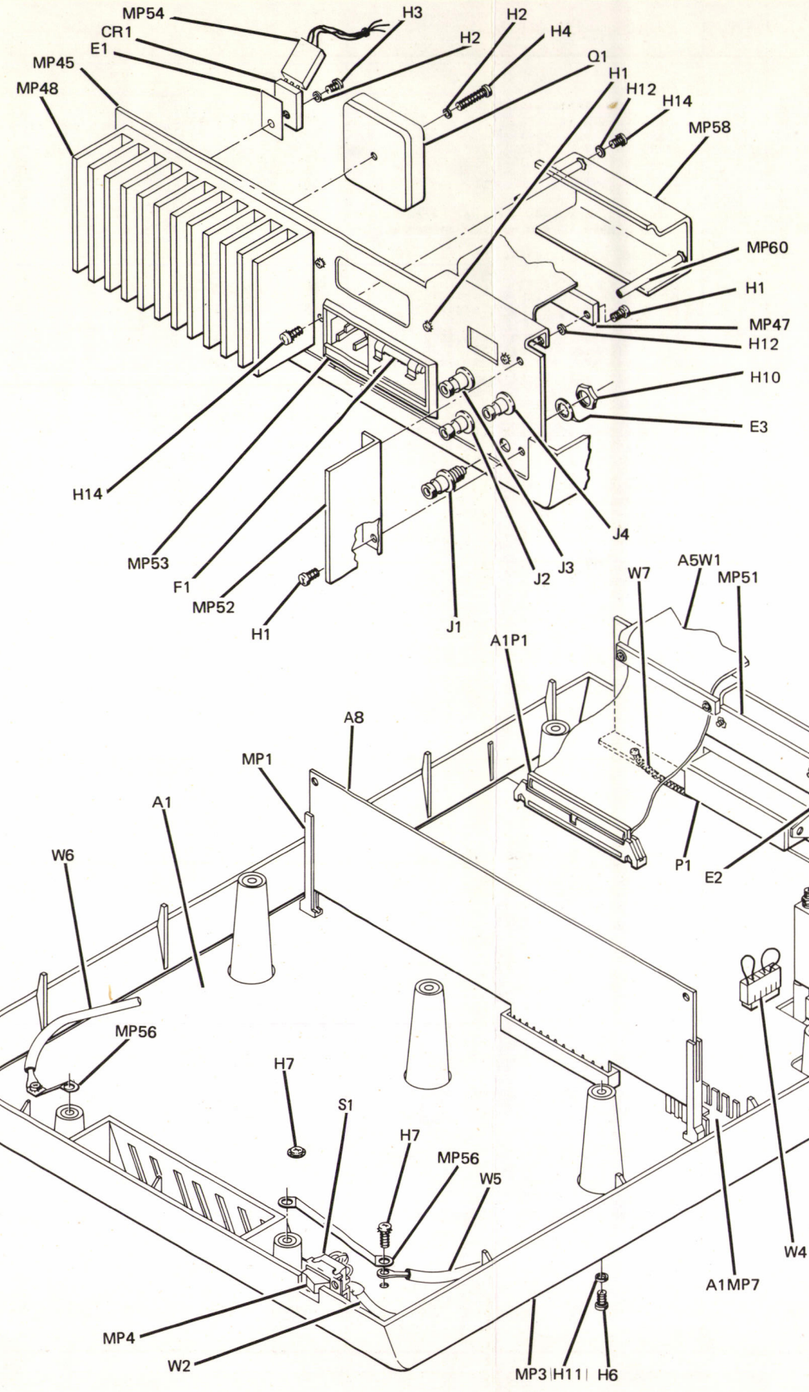
A	= assembly	**F**	= fuse	**MP**	= mechanical part	**U**	= integrated circuit
B	= motor	**FL**	= filter	**P**	= plug	**V**	= vacuum, tube, neon bulb, photocell, etc
BT	= battery	**IC**	= integrated circuit	**Q**	= transistor		
C	= capacitor	**J**	= jack	**R**	= resistor	**VR**	= voltage regulator
CP	= coupler	**K**	= relay	**RT**	= thermistor	**W**	= cable
CR	= diode	**L**	= inductor	**S**	= switch	**X**	= socket
DL	= delay line	**LS**	= loud speaker	**T**	= transformer	**Y**	= crystal
DS	= device signaling (lamp)	**M**	= meter	**TB**	= terminal board	**Z**	= tuned cavity network
E	= misc electronic part	**MK**	= microphone	**TP**	= test point		

ABBREVIATIONS

A	= amperes	**H**	= henries	**N/O**	= normally open	**RMO**	= rack mount only
AFC	= automatic frequency control	**HDW**	= hardware	**NOM**	= nominal	**RMS**	= root-mean square
AMPL	= amplifier	**HEX**	= hexagonal	**NPO**	= negative positive zero (zero temperature coefficient)	**RWV**	= reverse working voltage
		HG	= mercury				
BFO	= beat frequency oscillator	**HR**	= hour(s)				
BE CU	= beryllium copper	**HZ**	= hertz	**NPN**	= negative-positive-negative	**S-B**	= slow-blow
BH	= binder head					**SCR**	= screw
BP	= bandpass			**NRFR**	= not recommended for field replacement	**SE**	= selenium
BRS	= brass	**IF**	= intermediate freq			**SECT**	= section(s)
BWO	= backward wave oscillator	**IMPG**	= impregnated	**NSR**	= not separtely replaceable	**SEMICON**	= semiconductor
		INCD	= incandescent			**SI**	= silicon
CCW	= counter-clockwise	**INCL**	= include(s)			**SIL**	= silver
CER	= ceramic	**INS**	= insulation(ed)	**OBD**	= order by description	**SL**	= slide
CMO	= cabinet mount only	**INT**	= internal	**OH**	= oval head	**SPG**	= spring
COEF	= coeficient			**OX**	= oxide	**SPL**	= special
COM	= common	**K**	= kilo=1000			**SST**	= stainless steel
COMP	= composition					**SR**	= split ring
COMPL	= complete	**LH**	= left hand	**P**	= peak	**STL**	= steel
CONN	= connector	**LIN**	= linear taper	**PC**	= printed circuit		
CP	= cadmium plate	**LK WASH**	= lock washer	**PF**	= picofarads= 10^{-12} farads	**TA**	= tantalum
CRT	= cathode-ray tube	**LOG**	= logarithmic taper			**TD**	= time delay
CW	= clockwise	**LPF**	= low pass filter	**PH BRZ**	= phosphor bronze	**TGL**	= toggle
				PHL	= phillips	**THD**	= thread
DEPC	= deposited carbon	**M**	= milli=10^{-3}	**PIV**	= peak inverse voltage	**TI**	= titanium
DR	= drive	**MEG**	= meg=10^{6}	**PNP**	= positive-negative-positive	**TOL**	= tolerance
		MET FLM	= metal film			**TRIM**	= trimmer
ELECT	= electrolytic	**MET OX**	= metallic oxide	**P/O**	= part of	**TWT**	= traveling wae tube
ENCAP	= encapsulated	**MFR**	= manufacturer	**POLY**	= polystyrene		
EXT	= external	**MHZ**	= mega hertz	**PORC**	= porcelain	**U**	= micro=10^{-6}
		MINAT	= miniature	**POS**	= position(s)		
F	= farads	**MOM**	= momentary	**POT**	= potentiometer	**VAR**	= variable
FH	= flat head	**MOS**	= metal oxide substrate	**PP**	= peak-to-peak	**VDCW**	= dc working volts
FIL H	= fillister head	**MTG**	= mounting	**PT**	= point		
FXD	= fixed	**MY**	= "mylar"	**PWV**	= peak working voltage	**W/**	= with
						W	= watts
G	= giga (10^{9})	**N**	= nano (10^{-9})	**RECT**	= rectifier	**WIV**	= working inverse voltage
GE	= germanium	**N/C**	= normally closed	**RF**	= radio frequency		
GL	= glass	**NE**	= neon	**RH**	= round head or right hand	**WW**	= wirewound
GRD	= ground(ed)	**NI PL**	= nickel plate			**W/O**	= without







DETAIL
B

ROTATED
180°

SEE
DETAIL B

Figure 6-1.
Illustrated Parts Breakdown

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
			CHASSIS PARTS		
A1	01602-66501		BOARD ASSEMBLY, MAIN	28480	01602-66501
A2	01602-66502		BOARD ASSEMBLY, KEYBOARD	28480	01602-66502
A3	01602-66503		BOARD ASSEMBLY, DISPLAY	28480	01602-66503
A4	01602-66504		BOARD ASSEMBLY, HP-IB INTERFACE(OPT 001)	28480	01602-66504
A5	01602-62101		DATA PROBE ASSEMBLY	28480	01602-62101
A6	01602-62102		WIRE-ADAPTER, PROBE	28480	01602-62102
A7	01602-66507		BOARD ASSEMBLY, HP-IB CONNECTOR(OPT 001)	28480	01602-66507
A8	01602-66508		BOARD ASSEMBLY, ROM	28480	01602-66508
CR1	1906-0093	1	DIODE-FW BRDG 100V 35A	0203G	MDA3501
E1	0340-0511	1	INSULATOR-XSTR KAPTON	0260H	43-77-2
E2	0360-0009	1	TERMINAL-SLDR LUG PL-MTG FOR-#6-SCR	0460D	1912
E3	0360-1632	4	TERMINAL-SLDR LUG LK-MTG FOR-#3/8-SCR	79963	761-3/8
F1	2110-0202	1	FUSE .5A 250V SLO-BLO 1.25X.25 UL IEC (FOR 100-120V OPERATION)	0470C	313.500
F1	2110-0201	1	FUSE .25A 250V SLO-BLO 1.25X.25 UL IEC (FOR 220-240V OPERATION)	0470C	313.250
H1	2200-0103	22	SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI	28480	2200-0103
H2	2190-0910	2	WASHER-LK INTL T NO. 4 .12-IN-ID	0203G	04A52200F01
H3	2200-0141	1	SCREW-MACH 4-40 .312-IN-LG PAN-HD-POZI	28480	2200-0141
H4	2200-0151	1	SCREW-MACH 4-40 .75-IN-LG PAN-HD-POZI	28480	2200-0151
H5	2200-0165	4	SCREW-MACH 4-40 .25-IN-LG 82 DEG	28480	2200-0165
H6	2360-0117	8	SCREW-MACH 6-32 .375-IN-LG PAN-HD-POZI	28480	2360-0117
H7	2360-0115	19	SCREW-MACH 6-32 .312-IN-LG PAN-HD-POZI	28480	2360-0115
H8	2360-0139	4	SCREW-MACH 6-32 2-IN-LG PAN-HD-POZI	28480	2360-0139
H9	2420-0003	4	NUT-HEX-DBL-CHAM 6-32-THD .094-IN-THK	28480	2420-0003
H10	2950-0001	4	NUT-HEX-DBL-CHAM 3/8-32-THD .094-IN-THK	28480	2950-0001
H11	3050-0010	16	WASHER-FL MTLC NO. 6 .147-IN-ID	28480	3050-0010
H12	3050-0235	6	WASHER-FL MTLC NO. 4 .117-IN-ID	28480	3050-0235
H13	2190-0018	4	WASHER-LK HLCL NO. 6 .141-IN-ID	28480	2190-0018
H14	2200-0105	4	SCREW-MACH 4-40 .312-IN-LG PAN-HD-POZI	28480	2200-0105
J1	1250-0083	4	CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	0331F	28JR-130-1
J2	1250-0083		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	0331F	28JR-130-1
J3	1250-0083		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	0331F	28JR-130-1
J4	1250-0083		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	0331F	28JR-130-1
MP1	5040-0170	2	GUIDE;PLUG-IN PC BOARD	28480	5040-0170
MP2	5040-0571	1	CABINET-TOP	28480	5040-0571
MP3	5040-0572	1	CABINET-BOTTOM	28480	5040-0572
MP4	5040-7946	1	KEYCAP-LINE POWER ROCKER SWITCH	28480	5040-7946
MP5	5041-0050	1	KEYCAP-STOP	28480	5041-0050
MP6	5041-0051	1	KEYCAP-DON'T CARE	28480	5041-0051
MP7			NOT USED		
MP8	5041-0301	1	KEYCAP-BLANK	28480	5041-0301
MP9	5041-0631	1	KEYCAP-TRACE	28480	5041-0631
MP10	5041-0650	1	KEYCAP-BINARY	28480	5041-0650
MP11	5041-0651	1	KEYCAP-OCTAL	28480	5041-0651
MP12	5041-0652	1	KEYCAP-DECIMAL	28480	5041-0652
MP13	5041-0653	1	KEYCAP-HEX	28480	5041-0653
MP14	5041-0654	1	KEYCAP-CLOCK EDGE	28480	5041-0654
MP15	5041-0676	1	KEYCAP-1	28480	5041-0676
MP16	5041-0677	1	KEYCAP-2	28480	5041-0677
MP17	5041-0678	1	KEYCAP-3	28480	5041-0678
MP18	5041-0679	1	KEYCAP-4	28480	5041-0679
MP19	5041-0680	1	KEYCAP-5	28480	5041-0680
MP20	5041-0681	1	KEYCAP-6	28480	5041-0681
MP21	5041-0682	1	KEYCAP-7	28480	5041-0682
MP22	5041-0683	1	KEYCAP-8	28480	5041-0683
MP23	5041-0684	1	KEYCAP-9	28480	5041-0684
MP24	5041-0685	1	KEYCAP-0	28480	5041-0685
MP25	5041-0687	1	KEYCAP-CLEAR TRIG	28480	5041-0687
MP26			NOT USED		
MP27	5041-0759	1	KEYCAP-LOGIC POL	28480	5041-0759
MP28	5041-0760	1	KEYCAP-WORD WIDTH	28480	5041-0760
MP29	5041-0761	1	KEYCAP-DATA TRIG	28480	5041-0761
MP30	5041-0762	1	KEYCAP-WORD NUMBER	28480	5041-0762
MP31	5041-0763	1	KEYCAP-AT TRIG WORD	28480	5041-0763
MP32	5041-0764	1	KEYCAP-PRIOR WORD	28480	5041-0764
MP33	5041-0765	1	KEYCAP-NEXT WORD	28480	5041-0765
MP34	5041-0766	1	KEYCAP-TRIGGER	28480	5041-0766
MP35	5041-0767	1	KEYCAP-DELAY	28480	5041-0767
MP36	5041-0790	1	KEYCAP-A	28480	5041-0790
MP37	5041-0791	1	KEYCAP-B	28480	5041-0791
MP38	5041-0792	1	KEYCAP-C	28480	5041-0792
MP39	5041-0793	1	KEYCAP-D	28480	5041-0793
MP40	5041-0794	1	KEYCAP-E	28480	5041-0794

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
MP41	5041-0795	1	KEYCAP-F	28480	5041-0795
MP42	7120-6134	1	LABEL-INFORMATION 5.8-IN-WD 8.6-IN-LG (KEYBOARD FUNCTIONS, MESSAGE CODES)	28480	7120-6134
	7120-6467		LABEL-INFORMATION (FRENCH)	28480	7120-6467
	7120-6468		LABEL-INFORMATION (SPANISH)	28480	7120-6468
	7120-6469		LABEL-INFORMATION (ITALIAN)	28480	7120-6469
	7120-6697		LABEL-INFORMATION (JAPANESE)	28480	7120-6697
	7120-6960		LABEL-INFORMATION (GERMAN)	28480	7120-6960
MP43	7120-6135	1	NAMEPLATE .4-IN-WD 9.38-IN-LG AL	28480	7120-6135
MP44	01602-00201	1	PANEL, KEYBOARD	28480	01602-00201
MP45	01602-00202	1	PANEL, REAR	28480	01602-00202
MP46	01602-01201	1	BRACKET, DISPLAY	28480	01602-01201
MP47	01602-01202	1	CLAMP, STRAIN RELIEF	28480	01602-01202
MP48	01602-21101	1	HEAT SINK	28480	01602-21101
MP49	01602-28101	1	WINDOW, DISPLAY	28480	01602-28101
MP50	01602-64101	1	LID, STORAGE	28480	01602-64101
MP51	01602-64102	1	COVER, REAR PANEL(HP-IB HOLES)	28480	01602-64102
MP52	01602-64701	1	STAND, REAR PANEL	28480	01602-64701
MP53	01602-94301	1	LABEL, LINE VOLTAGE(FUSE REQUIREMENTS)	28480	01602-94301
MP54	01607-61612	1	CABLE, VOLTAGE REG, (CR1)	28480	01607-61612
MP55	0403-0179	4	FEET	28480	0403-0179
MP56	1460-1607	2	STRAP-GROUND	28480	1460-1607
MP57	01602-94302	3	LABEL-OPERATOR IDENTIFY DISPLAY	28480	01602-94302
MP58	4040-1345	1	COVER-LINE PWR RECEIPT PROTECTOR	28480	4040-1345
MP59	4342-0037	1	FELT STRIP	28480	4342-0037
MP60	0590-0935	2	STANDOFF-THREADED (4-40)	28480	0590-0935
P1	0960-0444	1	POWER MODULE, UNFILTERED	28480	0960-0444
Q1	1854-0558	1	TRANSISTOR NPN SI DARL PD=70W FT=1MHZ	28480	1854-0558
S1	3101-2080	1	SWITCH-RKR BASIC DPDT NS 3A 250VAC	28480	3101-2080
T1	9100-3996	1	TRANSFORMER, POWER	28480	9100-3996
W1	8120-1378	1	CABLE ASSY 18AWG 3-CNDCT JGK-JKT .25-OD (U,S,A,)	28480	8120-1378
W2	01602-61605	1	CABLE, LINE SWITCH	28480	01602-61605
W3	01602-61604	1	CABLE, DISPLAY (A3)	28480	01602-61604
W4	01602-61602	1	CABLE, POWER SUPPLY OUTPUT DISCONNECT	28480	01602-61602
W5	01602-61607	1	CABLE, GROUND (1,329 FT,)	28480	01602-61607
W6	01602-61608	1	CABLE, GROUND (1,696 FT,)	28480	01602-61608
W7	01602-61609	1	CABLE, GROUND (WIRE BRAID 0.125 FT.)	28480	01602-61609

See introduction to this section for ordering information

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1	01602-66501	1	BOARD ASSEMBLY, MAIN	28480	01602-66501
A1C1	0180-2762	1	CAPACITOR-FXD .01F+75-10% 15VDC AL	0546F	TCG103U15N3C3P
A1C2	0180-2763	1	CAPACITOR-FXD 2300UF+75-10% 25VDC AL	0546F	TCG232U025J2L3P
A1C3	0160-3451	8	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-3451
A1C4	0160-3451		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-3451
A1C5	0160-3508	11	CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A1C6	0140-0190	1	CAPACITOR-FXD 39PF +-5% 300VDC	72136	DM15E390J0300WV1CR
A1C7	0160-2101	4	CAPACITOR-FXD 27PF +-2% 300VDC	28480	0160-2101
A1C8	0160-2101		CAPACITOR-FXD 27PF +-2% 300VDC	28480	0160-2101
A1C9	0160-2307	1	CAPACITOR-FXD 47PF +-5% 300VDC	28480	0160-2307
A1C10	0160-3508		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A1C11	0160-2202	1	CAPACITOR-FXD 75PF +-5% 300VDC	28480	0160-2202
A1C12	0160-2101		CAPACITOR-FXD 27PF +-2% 300VDC	28480	0160-2101
A1C13	0180-0229	2	CAPACITOR-FXD 33UF+-10% 10VDC TA	0420J	150D336X9010B2
A1C14	0180-0229		CAPACITOR-FXD 33UF+-10% 10VDC TA	0420J	150D336X9010B2
A1C15	0180-0116	1	CAPACITOR-FXD 6.8UF+-10% 35VDC TA	0420J	150D685X9035B2
A1C16	0160-2101		CAPACITOR-FXD 27PF +-2% 300VDC	28480	0160-2101
A1C17	0160-3451		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-3451
A1C18	0160-3451		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-3451
A1C19	0160-3451		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-3451
A1C20	0160-3451		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-3451
A1C21	0160-3451		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-3451
A1C22	0160-3451		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-3451
A1C23	0160-3508		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A1C24	0160-3508		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A1C25	0160-3508		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A1C26	0160-3508		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A1C27	0160-3508		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A1C28	0160-3508		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A1C29	0160-3508		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A1C30	0160-3508		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A1C31	0160-3508		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A1CR1	1906-0006	1	DIODE-FW BRDG 400V 1A	28480	1906-0006
A1CR2	1901-0535	2	DIODE-SCHOTTKY	28480	1901-0535
A1CR3	1901-0535		DIODE-SCHOTTKY	28480	1901-0535
A1F1	2110-0003	1	FUSE 3A 250V FAST-BLO 1.25X.25 UL IEC	0470C	312003.
A1F2	2110-0012	1	FUSE .5A 250V FAST-BLO 1.25X.25 UL IEC	0470C	312.500
A1J1	1200-0474	1	SOCKET-IC 14-CONT DIP-SLDR	0325I	C8A-3100-14B
A1J2	1200-0473	1	SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0473
A1J3	1251-1626	1	CONNECTOR-PC EDGE 12-CONT/ROW 2-ROWS	0450G	252-12-30-300
A1L1	9100-1781	1	COIL-MLD 82UH 5% Q=42 .155DX.375LG	28480	9100-1781
A1MP1	2110-0269	4	FUSEHOLDER-CLIP TYPE .25D-FUSE	28480	2110-0269
A1MP2	2200-0143	1	SCREW-MACH 4-40 .375-IN-LG PAN-HD-POZI	28480	2200-0143
A1MP3	2260-0001	1	NUT-HEX-DBL-CHAM 4-40-THD .094-IN-THK	28480	2260-0001
A1MP4	3050-0235	1	WASHER-FL MTLC NO. 4 .117-IN-ID	28480	3050-0235
A1MP5	3050-0791	1	INSULATOR-XSTR NYLON	28480	3050-0791
A1MP6	2190-0019	1	WASHER-LK HLCL NO. 4 .115-IN-ID	28480	2190-0019
A1MP7	1205-0338	1	HEAT SINK	28480	1205-0338
A1MP8	1251-4045	2	SOCKET-GROUND (TEST POINT CUP)	28480	1251-4045
A1MP9	1400-0747	1	CABLE TIE .062-4-DIA. .184-WD NYL (CAPACITOR RESTRAINT)	59730	TY-28M-8
A1P1	1251-3004	1	CONNECTOR 40-PIN M RECTANGULAR	76381	3432-2002
A1P2	1251-0513	1	CONNECTOR 5-PIN M POST TYPE	27264	09-60-1051
A1Q1	1854-0628	2	TRANSISTOR NPN SI TO-92 PD=625MW	0203G	MPS-H17
A1Q2	1854-0628		TRANSISTOR NPN SI TO-92 PD=625MW	0203G	MPS-H17
A1R1	0698-3151	1	RESISTOR 2.87K 1% .125W F TC=0+-100	0329B	C4-1/8-T0-2871-F
A1R2	0757-0439	1	RESISTOR 6.81K 1% .125W F TC=0+-100	0329B	C4-1/8-T0-6811-F
A1R3	0684-1021	2	RESISTOR 1K 10% .25W FC TC=-400/+600	0160G	CB1021
A1R4	0757-0418	2	RESISTOR 619 1% .125W F TC=0+-100	0329B	C4-1/8-T0-619R-F
A1R5	0698-3447	2	RESISTOR 422 1% .125W F TC=0+-100	0329B	C4-1/8-T0-422R-F
A1R6	0684-2711	1	RESISTOR 270 10% .25W FC TC=-400/+600	0160G	CB2711
A1R7	0698-7923	2	RESISTOR 18 10% .125W CC TC=-270/+540	0160G	BB1801
A1R8	0757-0428	1	RESISTOR 1.62K 1% .125W F TC=0+-100	0329B	C4-1/8-T0-1621-F
A1R9	0684-2211	1	RESISTOR 220 10% .25W FC TC=-400/+600	0160G	CB2211
A1R10	0698-7923		RESISTOR 18 10% .125W CC TC=-270/+540	0160G	BB1801
A1R11	0757-0430	1	RESISTOR 2.21K 1% .125W F TC=0+-100	0329B	C4-1/8-T0-2211-F
A1R12	0684-4711	1	RESISTOR 470 10% .25W FC TC=-400/+600	0160G	CB4711
A1R13	0757-0442	2	RESISTOR 10K 1% .125W F TC=0+-100	0329B	C4-1/8-T0-1002-F
A1R14	0757-0442		RESISTOR 10K 1% .125W F TC=0+-100	0329B	C4-1/8-T0-1002-F
A1R15	0684-1021		RESISTOR 1K 10% .25W FC TC=-400/+600	0160G	CB1021

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1R16	0757-0418		RESISTOR 619 1% .125W F TC=0+-100	03298	C4-1/8-T0-619R-F
A1R17	0698-3447		RESISTOR 422 1% .125W F TC=0+-100	03298	C4-1/8-T0-422R-F
A1R18	0684-6821	1	RESISTOR 6.8K 10% .25W FC TC=-400/+700	0160G	CB6821
A1TP1	1251-2229	2	CONNECTOR-SGL CONT SKT .033-IN-BSC-SZ	0138J	1-331677-3
A1TP2	1251-2229		CONNECTOR-SGL CONT SKT .033-IN-BSC-SZ	0138J	1-331677-3
A1TP3	0360-0535	2	TERMINAL, TEST POINT	4G81I	OBD
A1TP4	0360-0535		TERMINAL, TEST POINT	4G81I	OBD
A1U1	1820-1430	6	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	0379D	AM74LS161N
A1U2	1816-1092	2	IC RAM TTL 256 X 1-BIT	28480	1816-1092
A1U3	1820-0691	4	IC GATE TTL S AND-OR-INV	0223G	74864PC
A1U4	1820-1475	4	IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	0223G	93816DC
A1U5	1820-1430		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	0379D	AM74LS161N
A1U6	1818-0316	1	IC PROGRAM STORAGE UNIT MOS	28480	1818-0316
A1U7	1816-0728	2	IC 82809I RAM TTL	0291J	82809I
A1U8	1820-0685	3	IC GATE TTL S NAND TPL 3-INP	0169M	SN74S10N
A1U9	1820-1475		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	0223G	93816DC
A1U10	1820-0685		IC GATE TTL S NAND TPL 3-INP	0169M	SN74S10N
A1U11	1820-1475		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	0223G	93816DC
A1U12	1820-1475		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	0223G	93816DC
A1U13	1820-0688	1	IC GATE TTL S NAND DUAL 4-INP	0223G	74820PC
A1U14	1818-0314	1	IC PROGRAM STORAGE UNIT MOS	28480	1818-0314
A1U15	1820-1130	1	IC GATE TTL S NAND 13-INP	0169M	SN748133N
A1U16	1816-0728		IC 82809I RAM TTL	0291J	82809I
A1U17	1820-1416	2	IC SCHMITT-TRIG TTL LS INV HEX 1-INP	0169M	SN74LS14N
A1U18	1820-0683	1	IC INV TTL S HEX 1-INP	0223G	74804PC
A1U19	1820-0691		IC GATE TTL S AND-OR-INV	0223G	74864PC
A1U20	1820-1416		IC SCHMITT-TRIG TTL LS INV HEX 1-INP	0169M	SN74LS14N
A1U21	1820-1199	2	IC INV TTL LS HEX 1-INP	0169M	SN74LS04N
A1U22	1820-1927	1	IC GATE TTL S AND QUAD	0223G	9841PC
A1U23	1816-1092		IC RAM TTL 256 X 1-BIT	28480	1816-1092
A1U24	1820-1282	1	IC FF TTL LS J-K BAR POS-EDGE-TRIG	0169M	SN74LS109N
A1U25	1820-0693	1	IC FF TTL S D-TYPE POS-EDGE-TRIG	0223G	74874PC
A1U26	1820-0691		IC GATE TTL S AND-OR-INV	0223G	74864PC
A1U27	1820-0691		IC GATE TTL S AND-OR-INV	0223G	74864PC
A1U28	1820-1372	2	IC FF TTL S J-K BAR CLEAR DUAL	0223G	748109DC
A1U29	1820-1372		IC FF TTL S J-K BAR CLEAR DUAL	0223G	748109DC
A1U30	1820-0685		IC GATE TTL S NAND TPL 3-INP	0169M	SN74S10N
A1U31	1826-0409	1	IC 723 V RGLTR	0223G	UA723DM
A1U32	1820-1425	1	IC SCHMITT-TRIG TTL LS NAND QUAD 2-INP	0169M	SN74LS132N
A1U33	1820-1156	1	IC GATE TTL S AND-OR-INV DUAL 2-INP	0169M	SN74S51N
A1U34	1820-0697	1	IC DRVR TTL S NAND LINE DUAL 4-INP	0223G	748140PC
A1U35	1820-1433	2	IC SHF-RGTR TTL LS R-S SERIAL-IN PRL OUT	0169M	SN74LS164N
A1U36	1820-1433		IC SHF-RGTR TTL LS R-S SERIAL-IN PRL OUT	0169M	SN74LS164N
A1U37	1820-1430		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	0379D	AM74LS161N
A1U38	1820-1430		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	0379D	AM74LS161N
A1U39	1820-1430		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	0379D	AM74LS161N
A1U40	1820-1430		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	0379D	AM74LS161N
A1U41	1820-1928	1	IC MICPROC MOS (CPU)	0407M	MK3850N-3
A1U42	1820-1199		IC INV TTL LS HEX 1-INP	0169M	SN74LS04N
A1U43	1820-1440	1	IC LCH TTL LS QUAD	0169M	SN74LS279N
A1U44	1826-0147	1	IC 7812 V RGLTR	0223G	7812UC
A1U45	1810-0305	2	NETWORK-RES 9-PIN-SIP .1-PIN-SPCG	0248C	750 SERIES
A1U46	1810-0305		NETWORK-RES 9-PIN-SIP .1-PIN-SPCG	0248C	750 SERIES
A1XU6	1200-0624	3	SOCKET-IC 40-CONT DIP-SLDR	82647	C934010
A1XU7	1200-0663	2	SOCKET-IC 28-CONT DIP-SLDR	0138J	530018-3
A1XU14	1200-0624		SOCKET-IC 40-CONT DIP-SLDR	82647	C934010
A1XU17	1200-0663		SOCKET-IC 28-CONT DIP-SLDR	0138J	530018-3
A1XU41	1200-0624		SOCKET-IC 40-CONT DIP-SLDR	82647	C934010
A2	01602-66502	1	BOARD ASSEMBLY, KEYBOARD	28480	01602-66502
A2C1	0170-0066	1	CAPACITOR-FXD .027UF +-10% 200VDC POLYE	0420J	292P27392
A2C2	0140-0198	2	CAPACITOR-FXD 200PF +-5% 300VDC MICA	72136	DM15F201J0300WV1CR
A2C3	0140-0198		CAPACITOR-FXD 200PF +-5% 300VDC MICA	72136	DM15F201J0300WV1CR
A2C4	0160-3443	3	CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A2C5	0160-3443		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A2C6	0160-3443		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A2C7	0160-3647	4	CAPACITOR-FXD 22PF +-5% 100VDC CER0+-30	28480	0160-3647
A2C8	0160-3647		CAPACITOR-FXD 22PF +-5% 100VDC CER0+-30	28480	0160-3647
A2C9	0160-3647		CAPACITOR-FXD 22PF +-5% 100VDC CER0+-30	28480	0160-3647
A2C10	0160-3647		CAPACITOR-FXD 22PF +-5% 100VDC CER0+-30	28480	0160-3647
A2CR1	1901-0025	3	DIODE-GEN PRP 100V 200MA DO-7	28480	1901-0025
A2CR2	1901-0025		DIODE-GEN PRP 100V 200MA DO-7	28480	1901-0025
A2CR3	1901-0025		DIODE-GEN PRP 100V 200MA DO-7	28480	1901-0025
A2D81	1990-0486	6	LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
A2D82	1990-0486		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
A2D83	1990-0486		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
A2D84	1990-0486		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
A2D85	1990-0486		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A2D86	1990-0486		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
A2H1	2360-0115	4	SCREW-MACH 6-32 .312-IN-LG PAN-HD-POZI	28480	2360-0115
A2MP1	01602-00203	1	PANEL, SUPPORT	28480	01602-00203
A2MP2	1460-1606	4	SPRING-CONTACT	28480	1460-1606
A2Q1	1854-0215	1	TRANSISTOR NPN SI PD=350MW FT=300MHZ	0203G	SPS 3611
A2Q2	1853-0036	1	TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A2R1	0684-4731	1	RESISTOR 47K 10% .25W FC TC=-400/+800	0160G	CB4731
A2R2	0684-5621	1	RESISTOR 5.6K 10% .25W FC TC=-400/+700	0160G	CB5621
A2R3	0684-6801	1	RESISTOR 68 10% .25W FC TC=-400/+500	0160G	CB6801
A2R4	0684-3321	1	RESISTOR 3.3K 10% .25W FC TC=-400/+700	0160G	CB3321
A2R5	0757-0416	1	RESISTOR 511 1% .125W F TC=0+-100	03298	C4-1/8-T0-511R-F
A2R6	0684-2711	1	RESISTOR 270 10% .25W FC TC=-400/+600	0160G	CB2711
A2R7	0757-0273	1	RESISTOR 3.01K 1% .125W F TC=0+-100	03298	C4-1/8-T0-3011-F
A2R8	0757-0440	1	RESISTOR 7.5K 1% .125W F TC=0+-100	03298	C4-1/8-T0-7501-F
A2R9	0757-0442	1	RESISTOR 10K 1% .125W F TC=0+-100	03298	C4-1/8-T0-1002-F
A2R10	0684-2211	6	RESISTOR 220 10% .25W FC TC=-400/+600	0160G	CB2211
A2R11	0684-2211		RESISTOR 220 10% .25W FC TC=-400/+600	0160G	CB2211
A2R12	0684-2211		RESISTOR 220 10% .25W FC TC=-400/+600	0160G	CB2211
A2R13	0684-2211		RESISTOR 220 10% .25W FC TC=-400/+600	0160G	CB2211
A2R14	0684-2211		RESISTOR 220 10% .25W FC TC=-400/+600	0160G	CB2211
A2R15	0684-2211		RESISTOR 220 10% .25W FC TC=-400/+600	0160G	CB2211
A2S1-A2S39	3101-2137	39	SWITCH-PB SPST-NO MOM	28480	3101-2137
A2U1	1820-1429	1	IC CNTR TTL LS DECD SYNCHRO	0379D	AM74L8160N
A2U2	1820-0174	1	IC INV TTL HEX 1-INP	0223G	7404PC
A2U3	1821-0002	1	TRANSISTOR ARRAY	0192A	CA3045
A2U4	1820-1426	1	IC DCDR TTL LS BCD-TO-DEC 4-TO-10-LINE	0169H	SN74L8145N
A2U5	1810-0303	1	NETWORK-RES 8-PIN-SIP .1-PIN-SPCG	28480	1810-0303
A2U6	1810-0304	1	NETWORK-RES 6-PIN-SIP .1-PIN-SPCG	0248C	750-61-R1K
A2W1	01602-61603	1	CABLE, KEYBOARD	28480	01602-61603
A2XD81-A2XD86	5061-1249	6	SOCKET-LED (2 PIN)	28480	5061-1249
A3	01602-66503	1	BOARD ASSEMBLY, DISPLAY (NOTE: DISPLAY CABLE W3, 01602-61604 NOT INCLUDED)	28480	01602-66503
A3C1	0180-0229	1	CAPACITOR-FXD 33UF+-10% 10VDC TA	0420J	150D336X901082
A3C2	0180-0116	1	CAPACITOR-FXD 6.8UF+-10% 35VDC TA	0420J	150D685X903582
A3D81	1990-0618	4	LED-VISIBLE LUM-INT=800UCD IF=60MA-MAX	28480	1990-0618
A3D82	1990-0618		LED-VISIBLE LUM-INT=800UCD IF=60MA-MAX	28480	1990-0618
A3D83	1990-0618		LED-VISIBLE LUM-INT=800UCD IF=60MA-MAX	28480	1990-0618
A3D84	1990-0618		LED-VISIBLE LUM-INT=800UCD IF=60MA-MAX	28480	1990-0618
A3R1	0684-1011	2	RESISTOR 100 10% .25W FC TC=-400/+500	0160G	CB1011
A3R2	0684-1011		RESISTOR 100 10% .25W FC TC=-400/+500	0160G	CB1011
A3R3	0684-6821	1	RESISTOR 6.8K 10% .25W FC TC=-400/+700	0160G	CB6821
A3U1	1858-0058	2	TRANSISTOR ARRAY 14-PIN PLSTC TO-116	0203G	MPQ3906
A3U2-A3U19	1990-0619	18	DISPLAY-NUM SEG 1-CHAR .3-H GA-ARSD-PPMD	28480	1990-0619
A3U20	1858-0058		TRANSISTOR ARRAY 14-PIN PLSTC TO-116	0203G	MPQ3906
A3U21	1820-1199	2	IC INV TTL LS HEX 1-INP	0169H	SN74L804N
A3U22	1820-1231	3	IC DRVR MOS HEX 1-INP	0203G	MC75492P
A3U23	1820-1196	3	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	0379D	AM74L8174N
A3U24	1820-1231		IC DRVR MOS HEX 1-INP	0203G	MC75492P
A3U25	1820-1196		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	0379D	AM74L8174N
A3U26	1820-1231		IC DRVR MOS HEX 1-INP	0203G	MC75492P
A3U27	1820-1196		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	0379D	AM74L8174N
A3U28	1810-0306	1	NETWORK-RES 16-PIN-DIP .1-PIN-SPCG	28480	1810-0306
A3U29	1820-1199		IC INV TTL LS HEX 1-INP	0169H	SN74L804N
A3U30	1810-0302	2	NETWORK-RES 8-PIN-SIP .1-PIN-SPCG	28480	1810-0302
A3U31	1810-0302		NETWORK-RES 8-PIN-SIP .1-PIN-SPCG	28480	1810-0302
A4			LISTED UNDER OPTION 001 (AT END OF REPLACEABLE PARTS LIST)		

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A5	01602-62101	1	DATA PROBE ASSEMBLY NOTE: BOARD ASSY A5A1 AND PROBE CABLE A5W1 ARE NOT SOLD SEPARATELY. TO OBTAIN REPLACEMENTS, THE ENTIRE DATA PROBE ASSY (01602-62101) MUST BE ORDERED.	28480	01602-62101
A5H1	0624-0306	4	SCREW-TPG 2-28 .5-IN-LG PAN-HD-POZI STL	28480	0624-0306
A5MP1	5040-8208	1	PROBE COVER-BOTTOM	28480	5040-8208
A5MP2	5040-8209	1	PROBE COVER-TOP	28480	5040-8209
A5MP3	7120-6133	1	LABEL-PROBE	28480	7120-6133
A5A1C1	0180-0229	1	CAPACITOR-FXD 33UF+-10% 10VDC TA	0420J	150D336X9010B2
A5A1C2	0160-3443	5	CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5A1C3	0160-3443		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5A1C4	0160-3443		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5A1C5	0160-3443		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5A1C6	0160-3443		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5A1J1	1251-4792	1	CONNECTOR-PC EDGE 20-CONT/ROW 2-ROWS	28480	1251-4792
A5A1R1	0698-3378	2	RESISTOR 51 5% .125W CC TC=-270/+540	0160G	BB5105
A5A1R2	0698-3378		RESISTOR 51 5% .125W CC TC=-270/+540	0160G	BB5105
A5A1R3	0698-6750	1	RESISTOR 220K 10% .125W CC TC=-600/+1137	0160G	BB2241
A5A1U1	1810-0301	2	NETWORK-RES 16-PIN-DIP .1-PIN-SPCG	28480	1810-0301
A5A1U2	1820-1924	3	IC INV TTL 8 HEX	0291J	8T93A
A5A1U3	1820-1139	6	IC:TTL, HEX INVERTER	28480	1820-1139
A5A1U4	1820-1139		IC:TTL, HEX INVERTER	28480	1820-1139
A5A1U5	1820-1924		IC INV TTL 8 HEX	0291J	8T93A
A5A1U6	1820-1139		IC:TTL, HEX INVERTER	28480	1820-1139
A5A1U7	1820-1139		IC:TTL, HEX INVERTER	28480	1820-1139
A5A1U8	1810-0301		NETWORK-RES 16-PIN-DIP .1-PIN-SPCG	28480	1810-0301
A5A1U9	1820-1924		IC INV TTL 8 HEX	0291J	8T93A
A5A1U10	1820-1139		IC:TTL, HEX INVERTER	28480	1820-1139
A5A1U11	1820-1139		IC:TTL, HEX INVERTER	28480	1820-1139
A6	01602-62102	1	WIRE-ADAPTER, PROBE	28480	01602-62102
A6CP1-A6CP18	10230-62101	18	PROBE ASSEMBLY, HOOK TYPE	28480	10230-62101
A6H1	0620-0390	2	SCREW-TPG 2-28 0.625-IN-LG PAN-HD-POZI STL	28480	0620-0390
A6MP1	5040-8206	1	COVER-TOP	28480	5040-8206
A6MP2	5040-8207	1	COVER-BOTTOM	28480	5040-8207
A6MP3	7120-6152	1	LABEL-INFORMATION .755-IN-WD 2.48-IN-LG	28480	7120-6152
A6A1	01602-66506	1	BOARD ASSEMBLY, INTERFACE ADAPTER	28480	01602-66506
A6A1W1	5061-1231	1	CABLE-PIN ADAPTER, BLACK	28480	5061-1231
A6A1W2	5061-1232	1	CABLE-PIN ADAPTER, YELLOW	28480	5061-1232
A6A1W3	5061-1233	1	CABLE-PIN ADAPTER, WHITE/BLACK	28480	5061-1233
A6A1W4	5061-1234	1	CABLE-PIN ADAPTER, WHITE/BROWN	28480	5061-1234
A6A1W5	5061-1235	1	CABLE-PIN ADAPTER, WHITE/RED	28480	5061-1235
A6A1W6	5061-1236	1	CABLE-PIN ADAPTER, WHITE/ORANGE	28480	5061-1236
A6A1W7	5061-1237	1	CABLE-PIN ADAPTER, WHITE/YELLOW	28480	5061-1237
A6A1W8	5061-1238	1	CABLE-PIN ADAPTER, WHITE/GREEN	28480	5061-1238
A6A1W9	5061-1239	1	CABLE-PIN ADAPTER, WHITE/BLUE	28480	5061-1239
A6A1W10	5061-1240	1	CABLE-PIN ADAPTER, WHITE/VIOLET	28480	5061-1240
A6A1W11	5061-1241	1	CABLE-PIN ADAPTER, GRAY/BLACK	28480	5061-1241
A6A1W12	5061-1242	1	CABLE-PIN ADAPTER, GRAY/BROWN	28480	5061-1242
A6A1W13	5061-1243	1	CABLE-PIN ADAPTER, GRAY/RED	28480	5061-1243
A6A1W14	5061-1244	1	CABLE-PIN ADAPTER, GRAY/ORANGE	28480	5061-1244
A6A1W15	5061-1245	1	CABLE-PIN ADAPTER, GRAY/YELLOW	28480	5061-1245
A6A1W16	5061-1246	1	CABLE-PIN ADAPTER, GRAY/GREEN	28480	5061-1246
A6A1W17	5061-1247	1	CABLE-PIN ADAPTER, GRAY/BLUE	28480	5061-1247
A6A1W18	5061-1248	1	CABLE-PIN ADAPTER, GRAY/VIOLET	28480	5061-1248
A7			LISTED UNDER OPTION 001 (AT END OF REPLACEABLE PARTS LIST)		

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A8	01602-66508	1	BOARD ASSEMBLY, ROM	28480	01602-66508
A8C1	0160-3451	2	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-3451
A8C2	0160-3451		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-3451
A8U1	1818-0359	1	IC PROGRAM STORAGE UNIT MOS (SELF-TEST)	28480	1818-0359
A8XU1	1200-0624	1	SOCKET-IC 40-CONT DIP-SLDR	82647	C934010

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
			OPTION 001 (HP-IB)		
			DELETE: A8 ROM BOARD (01602-66508) MP51 HP-IB REAR PANEL HOLE COVER (01602-64102) MP9 KEYCAP-TRACE (5041-0631) MP5 KEYCAP-STOP (5041-0050)		
			ADD THE FOLLOWING PARTS:		
A4	01602-66504	1	BOARD ASSEMBLY, HP-IB INTERFACE		
A4C1	0180-0229	1	CAPACITOR-FXD 33UF+-10% 10VDC TA	0420J	150D336X9010B2
A4C2	0140-0149	1	CAPACITOR-FXD 470PF +-5% 300VDC MICA	72136	DM15F471J0300WV1CR
A4C3	0160-3450	1	CAPACITOR-FXD 5000PF +-10% 250VDC CER	28480	0160-3450
A4C4	0160-3451	3	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-3451
A4C5	0160-3451		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-3451
A4C6	0160-3451		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-3451
A4J1	1251-3024	1	CONNECTOR 26-PIN M RECTANGULAR	76381	3429-2002
A4Q1	1854-0071	1	TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A4R1	1810-0136	1	NETWORK-RES 10-PIN-SIP .1-PIN-SPCG	28480	1810-0136
A4R2	0757-0437	6	RESISTOR 4.75K 1% .125W F TC=0+-100	03298	C4-1/8-T0-4751-F
A4R3	0757-0437		RESISTOR 4.75K 1% .125W F TC=0+-100	03298	C4-1/8-T0-4751-F
A4R4	0757-0437		RESISTOR 4.75K 1% .125W F TC=0+-100	03298	C4-1/8-T0-4751-F
A4R5	0757-0437		RESISTOR 4.75K 1% .125W F TC=0+-100	03298	C4-1/8-T0-4751-F
A4R6	0757-0437		RESISTOR 4.75K 1% .125W F TC=0+-100	03298	C4-1/8-T0-4751-F
A4R7	0757-0437		RESISTOR 4.75K 1% .125W F TC=0+-100	03298	C4-1/8-T0-4751-F
A4U1	1820-1197	1	IC GATE TTL LS NAND QUAD 2-INP	0169H	SN74LS00N
A4U2	1820-1112	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG	0169H	SN74LS74N
A4U3	1820-1440	1	IC LCH TTL LS QUAD	0169H	SN74LS279N
A4U4	1820-1202	1	IC GATE TTL LS NAND TPL 3-INP	0223G	9L810PC
A4U5	1820-1281	1	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	0379D	AM74LS139
A4U6	1820-1216	1	IC DCDR TTL LS 3-TO-8-LINE 1-INP	0379D	SN74LS138N
A4U7	1820-1416	1	IC SCHMITT-TRIG TTL LS INV HEX 1-INP	0169H	SN74LS14N
A4U8	1820-1210	2	IC GATE TTL LS AND-OR-INV DUAL 2-INP	0169H	SN74LS51N
A4U9	1818-0358	1	IC PROGRAM STORAGE UNIT MOS	28480	1818-0358
A4U10	1820-1997	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	0379D	SN74LS374PC
A4U11	1820-1689	3	IC MISC QUAD	0203G	MC3446P
A4U12	1820-1689		IC MISC QUAD	0203G	MC3446P
A4U13	1820-1905	1	IC GATE TTL LS NOR DUAL 5-INP	0291J	N74LS260A
A4U14	1820-1201	1	IC GATE TTL LS AND QUAD 2-INP	0169H	SN74LS08N
A4U15	1820-1272	1	IC BFR TTL LS NOR QUAD 2-INP	0169H	SN74LS33N
A4U16	1818-0359	1	IC PROGRAM STORAGE UNIT MOS (SELF-TEST)	28480	1818-0359
A4U17	1820-1689		IC MISC QUAD	0203G	MC3446P
A4U18	1820-0904	1	IC COMPTR TTL L MAGTD 5-BIT	0223G	93L24PC
A4U19	1820-1210		IC GATE TTL LS AND-OR-INV DUAL 2-INP	0169H	SN74LS51N
A4U20	1820-1282	1	IC FF TTL LS J-K BAR POS-EDGE-TRIG	0169H	SN74LS109N
A4XU9	1200-0624	2	SOCKET-IC 40-CONT DIP-SLDR	82647	C934010
A4XU16	1200-0624		SOCKET-IC 40-CONT DIP-SLDR	82647	C934010
A7	01602-66507	1	BOARD ASSEMBLY, HP-IB CONNECTOR	28480	01602-66507
			NOTE: HP-IB CONNECTOR RECEPTACLE A7J1 AND CABLE ASSY A7W1 ARE NOT SOLD SEPARATELY. TO OBTAIN REPLACEMENTS, THE ENTIRE A7 BOARD ASSY (01602-66507) MUST BE ORDERED.		
A7S1	3101-2197	1	SWITCH-RKR DIP-RKR-ASSY 6-1A NS .5A	28480	3101-2197
	0380-0643	2	STANDOFF, LG STUD MOUNT(METRIC THREAD)	0046A	OBD#
	2200-0103	1	SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI	28480	2200-0103
	5041-0072	1	KEYCAP-TRACE, RETURN TO LOCAL	28480	5041-0072
	5041-0722	1	KEYCAP-STOP, PRINT	28480	5041-0722
	5951-2623	1	LABEL-OPT 001 IDENT	28480	5951-2623

See introduction to this section for ordering information

Table 6-3. List of Manufacturers' Codes

Mfr No.	Manufacturer Name	Address		Zip Code
0138J	AMP INC	HARRISBURG	PA	17105
0160G	ALLEN–BRADLEY CO	MILWAUKEE	WI	53212
0169H	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75231
0192A	RCA CORP SOLID STATE DIV	SOMERVILLE	NJ	08876
0203G	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85008
0223G	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94040
0248C	CTS OF BERNE INC	BERNE	IN	46711
0260H	THERMALLOY CO	DALLAS	TX	75247
0291J	SIGNETICS CORP	SUNNYVALE	CA	94086
0325I	STANFORD APPLIED ENGINEERING INC	SANTA CLARA	CA	95050
0329B	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
0331F	SPECIALTY CONNECTOR CO INC	INDIANAPOLIS	IN	46227
27264	MOLEX PRODUCTS CO	DOWNERS GROVE	IL	60515
28480	HP DIV 00 CORPORATE	PALO ALTO	CA	94304
28520	HEYMAN MFG CO	KENILWORTH	NJ	07033
0379D	ADVANCED MICRO DEVICES INC	SUNNYVALE	CA	94086
0407H	MOSTEK CORP	CARROLLTON	TX	75006
0420J	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
59730	THOMAS & BETTS CO THE	ELIZABETH	NJ	07207
0450G	TRW ELEK COMPONENTS CINCH DIV	ELK GROVE VLGE	IL	60007
72136	ELECTRO MOTIVE CORP SUB IEC	WILLIMANTIC	CT	06226
0460D	FEDERAL SCREW PRODUCTS CO	CHICAGO	IL	60618
0470C	LITTELFUSE INC	DES PLAINES	IL	60016
76381	3M COMPANY	ST PAUL	MN	55101
79963	ZIERICK MFG CO	MT KISCO	NY	10549
82647	TEXAS INST DEPT CONTROL PROD DIV	ATTLEBORO	MA	02703
0546F	MALLORY CAPACITOR CO	INDIANAPOLIS	IN	46206

See introduction to this section for ordering information

SECTION VII

MANUAL CHANGES

This section normally contains information for adapting this manual to instruments for which the content does not apply directly. Since this manual does apply directly to insruments having serial numbers listed on the title page, no change information is given here. Refer to INSTRUMENTS COVERED BY MANUAL in Section I for additional important information about serial number coverage.

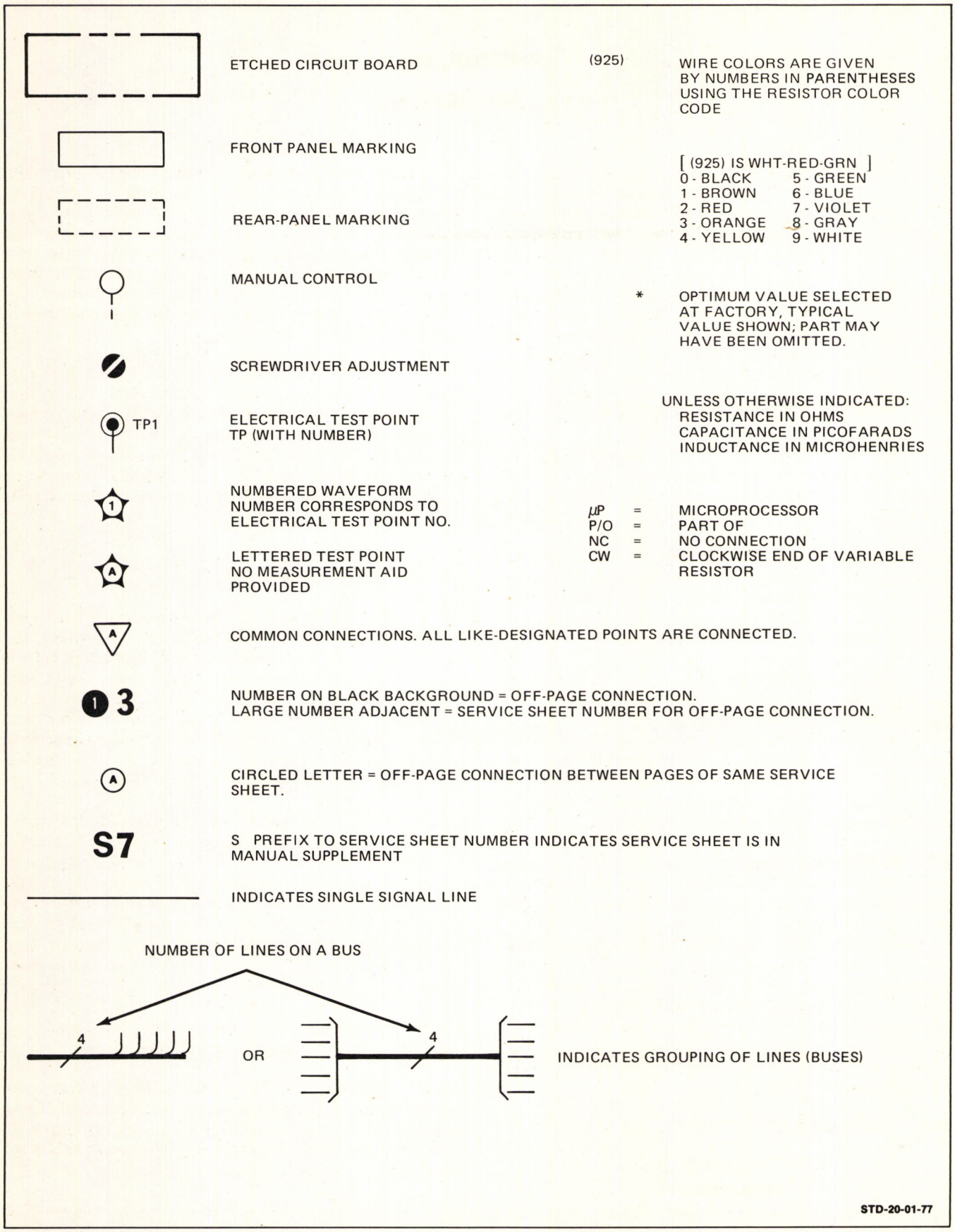


Figure 8-1. Schematic Diagram Notes

SECTION VIII

SERVICE

8-1. INTRODUCTION.

8-2. This section contains instructions for troubleshooting and repairing the Hewlett-Packard Model 1602A Logic State Analyzer.

8-3. Principles of operation and troubleshooting information are located opposite the schematics on fold-out Service Sheets. The rest of this section has general service information that should help you to quickly service and repair the 1602A.

8-4. PRINCIPLES OF OPERATION.

8-5. Principles of operation appear on pages opposite the block diagram and schematics on the Service Sheets. Figure 8-1 explains symbols that appear on the schematics. Figure 8-3 is an overall block diagram that briefly describes overall instrument operation. It is keyed, by Service Sheet numbers in the blocks, to schematics on the Service Sheets. These Service Sheets provide a stage-by-stage description of circuits on the schematics. The stages are keyed to the descriptions by stage names that appear on the schematics.

8-6. LOGIC CONVENTIONS. Positive logic convention is used in describing logic variables and circuits within the 1602A. Positive logic convention defines a logic "1" as the more positive voltage (high) and a logic "0" as the more negative voltage (low). The integrated circuits in the 1602A are almost entirely transistor-transistor-logic (TTL). Major exceptions are the MOS integrated circuits associated with the F8 microprocessor.

8-7. MNEMONICS. Signals in the 1602A have been assigned mnemonics that describe the active state and function of the signal line. A prefix letter (H, L, P, or N) indicates the active state of the signal, and the remaining letters indicate its function. An H prefix indicates the function is active in the high state; an L prefix indicates the function is active in the low state. For edge-controlled devices, the prefix P indicates the function is active on the positive-going transition; prefix N indicates the function is active on the negative-going transition. Mnemonic functional definitions are listed alphabetically in table 8-5.

8-8. TROUBLESHOOTING.

WARNING

Read the Safety Summary at the front of this manual before troubleshooting the instrument.

8-9. The most important prerequisites for successful troubleshooting are an understanding of instrument functional operation and the correct use of front panel controls. Suspected malfunctions may be caused by improper control settings. Before troubleshooting, refer to Section III (Operation) for an explanation of controls, connectors, and general operating considerations, and to the service sheets in this section for an explanation of circuit functional operation.

8-10. If trouble is suspected, visually inspect the instrument. Look for loose or burned components that might suggest a source of trouble. Verify that all circuit board connections are making good contact and are not shorting to an adjacent circuit. If no obvious trouble is found, check the instrument power-supply voltages and external power sources. A troubleshooting flow chart is shown in figure 8-2.

8-11. SELF-TEST.

8-12. The 1602A self-test feature provides both verification and diagnostic capabilities. At turn-on, the self-test automatically checks RAM, ROM, and I/O. It also checks the trigger recognition, delay, start/end, logic polarity and clock slope circuits. If a failure occurs during self-test, the 1602A will record the error and complete the test. Error message "E99" will then appear on the display. Pressing any key except "d" will initiate a lamp verification test displaying all "8's."

8-13. Pressing "d" causes self-test to repeat. It stops on the first failure and a detailed readout of the test segment is displayed. An "E" number is assigned to each test segment. Various test parameters may appear in the display. Pressing any key steps the self-test to the next test segment. The 1602A then runs through the test sequence until the next failure is detected. By observing error messages and test parameters, the failed circuits or components can be located.

8-14. When self-test is successfully completed, the instrument can be used in normal operation.

8-15. TEST PARAMETERS. Displayed test parameters (P numbers) are two-digit hexadecimal numbers. They appear on the display in the positions shown below. (P numbers are significant only if referenced in tables 8-1 and 8-2.)

P1	E**	P4	P3	P2

8-16. Table 8-1 lists error messages relating to memory and I/O port failures. For I/O port tests, P1 indicates which I/O bit(s) failed during self-test. P1 is formatted as shown below. P1 is the exclusive OR of what should be on the I/O port and the actual value. Thus faults are indicated by bits with a "1" value. For example, P1 = 40 (0100 0000) indicates that bit 6 failed the test. Table 8-3 lists bit assignments for each I/O port.

Bit 7	Bit 6	Bit 5	Bit 4

Bit 3	Bit 2	Bit 1	Bit 0

8-17. Table 8-2 lists error messages relating to the functional self-test. During functional self-test, the instrument sets up front-panel controls and generates data internally to check functional operation. For these tests, P1 shows the data word number (3F → 0) on the 1602A where the error occurred. P2 shows upper data memory fault position (8 MSB of data word stored in U16) and P3 shows lower data memory fault position (8 LSB of data word stored in U7). P4 shows the exclusive OR of expected values and actual values of the memory address count (MA0-MA5), HTP, and HMF. As with the P numbers in table 8-1, faults are indicated by bits in the 1 state. Refer to table 8-3 for data memory (I/O Port 8) and memory address count, HTP, and HMF (I/O Port 9) bit assignments. Table 8-4 lists examples of observed error messages and their probable causes.

8-18. KEYBOARD TEST.

8-19. The keyboard test is initiated by pressing the C key when power is applied. P1 will be "1." The rest of the display is blanked. Keys are numbered consecutively 1 to 35 from top to bottom, left to right. At each step in the test, "P1" indicates the next key to be pressed. If the expected key is pressed, "P1" increments to the next key position. "E98" blinks when an incorrect key sequence steps "P1" to the next key position. "P2" indicates key number of keycode received by the microprocessor. An invalid key code results in "P1" = 0. Refer to the keyboard test description in Section III for more information.

Table 8-1. Memory/IO Self-Test Failures

ERROR MESSAGE	TEST MODE	COMMENTS
E97	RAM	CPU RAM failure (A1U41)
E60	ROM Checksum	P1 = Checksum residue P2 = ROM fault page number 0 = A8U1 1 = A1U14 2 = A1U6
E61 E62 E63 E64 E65	I/O PORT 4 (A1U14) I/O PORT 5 (A1U14) I/O PORT 1 (A1U41) I/O PORT 0 (A1U41) I/O PORT 9 (A1U6)	P1 shows fault location (bit number)
E67	TMU and TML Both High (All I/O PORT 8 inputs should be high)	P1 shows fault location This test checks I/O Port 8 (A1U6) and high-speed memory (A1U16, A1U7)
E66	HCT High	P1 shows fault location If P1 = 08, check A1U24A. P1 = 10, check A1U28A. P1 = 18, check A1U17A.

Table 8-2. Functional Self-test Failures

Error Message	Trigger (A1U4, U9, U11, U12, U2, U23, U22B, U15, U28B)	Delay (A1U35-U40, U15, U22C)	Trace Starts/Ends (A1U10A)	Logic Polarity (A1U14)	Clock Slope (A1U19/U26)
E70	Dont't Care	0	start	Neg	Pos
E71	0000	0	start	Neg	Pos
E72	0F0F	0	start	Pos	Pos
E73	F0F0	0	start	Pos	Neg
E74	0000	15 (U37)	start	Neg	Pos
E75	0000	240 (U37, 38)	start	Neg	Neg
E76	0000	3840 (U37-40)	start	Pos	Pos
E77	0000	61440 (U37-40)	start	Pos	Neg
E78	Don't Care	0	end	Neg	Pos
E79	0F0F	0	end	Neg	Neg
E80	F0F0	0	end	Pos	Pos
E81	0000	15 (U37)	end	Pos	Neg
E82	0000	240 (U37, 38)	end	Neg	Pos
E83	0000	3840 (U37-40)	end	Neg	Neg
E84	0000	65535 (U37-40)	end	Pos	Pos
E85	AAAA	15 EVENTS (U30B)	start	Pos	Neg
E86	5555	15 EVENTS	end	Neg	Pos
E87	AAAA	0	start EVENTS (U21A, 21B, U27)	Neg	Neg
E88	5555	0	start EVENTS	Pos	Pos
E89	5555	0	end EVENTS	Pos	Neg
E90	5555	10	start EVENTS	Neg	Pos
E91	AAAA	4 EVENTS (U30B)	end EVENTS	Neg	Neg

Table 8-3. I/O Port Assignments

I/O PORT	PIN NO.	PIN LABEL	SIGNAL	P NUMBER BIT ASSIGNMENT	COMMENTS
0	U41, 16	$\overline{\text{I/O 00}}$	g	0	LED segment control High level lights segment.
	U41, 11	$\overline{\text{I/O 01}}$	f	1	
	U41, 10	$\overline{\text{I/O 02}}$	e	2	
	U41, 5	$\overline{\text{I/O 03}}$	d	3	
	U41, 36	$\overline{\text{I/O 04}}$	c	4	
	U41, 31	$\overline{\text{I/O 05}}$	b	5	
	U41, 30	$\overline{\text{I/O 06}}$	a	6	
	U41, 25	$\overline{\text{I/O 07}}$	NDSPCK	7	Negative Transition advance display register.

Table 8-3. I/O Port Assignments (Cont'd)

I/O PORT	PIN NO.	PIN LABEL	SIGNAL	P NUMBER BIT ASSIGNMENT	COMMENTS
1	U41, 14	$\overline{\text{I/O 10}}$	HKYD	0	High=Key Depressed previous scan
	U41, 13	$\overline{\text{I/O 11}}$	HSTRB	1	High loads trace into display register.
	U41, 8	$\overline{\text{I/O 12}}$	HCLP	2	High=Clock Present.
	U41, 7	$\overline{\text{I/O 13}}$	HQLP	3	High=Clock Qualifier Present.
	U41, 34	$\overline{\text{I/O 14}}$	$\overline{\text{C4}}$	4	From keyboard. High=key depressed.
	U41, 33	$\overline{\text{I/O 15}}$	$\overline{\text{C3}}$	5	
	U41, 28	$\overline{\text{I/O 16}}$	$\overline{\text{C2}}$	6	
	U41, 27	$\overline{\text{I/O 17}}$	$\overline{\text{C1}}$	7	
4	U14, 19	$\overline{\text{I/O A0}}$	HRTE	0	High, Record Trigger Events.
	U14, 24	$\overline{\text{I/O A1}}$	LST	1	Low, Self-Test.
	U14, 25	$\overline{\text{I/O A2}}$	HITA	2	High, Enable Trigger Address Counter Increment.
	U14, 30	$\overline{\text{I/O A3}}$	HSTOP	3	High, Stop.
	U14, 31	$\overline{\text{I/O A4}}$	LDBE	4	Low, Delay By Events.
	U14, 36	$\overline{\text{I/O A5}}$	HPCL	5	High, Positive Clock Slope.
	U14, 37	$\overline{\text{I/O A6}}$	HPLOG	6	High, Positive Logic Polarity.
	U14, 2	$\overline{\text{I/O A7}}$	HSTART	7	High, Start on Trigger
5	U14, 20	$\overline{\text{I/O B0}}$	PITA	0	Positive, Increment Trigger Address Counters
	U14, 23	$\overline{\text{I/O B1}}$	TML	1	Trigger Memory Lower. High=zero delay, low=select upper Data Memory data, match lower trigger
	U14, 26	$\overline{\text{I/O B2}}$	TMU	2	Trigger Memory Upper. Low=select lower Data Memory data, match upper trigger
	U14, 29	$\overline{\text{I/O B3}}$	HCTA	3	High, Clear Trigger Address Counters
	U14, 32	$\overline{\text{I/O B4}}$	PDRC	4	Positive, Delay Control Register Clock
	U14, 35	$\overline{\text{I/O B5}}$	NIMA	5	Negative, increment memory address counter.
	U14, 38	$\overline{\text{I/O B6}}$	LRES	6	Low, Reset.
	U14, 1	$\overline{\text{I/O B7}}$	HCT	7	High, Clear CLK and CLK Qual Present Tests
8	U6, 19	$\overline{\text{I/O A0}}$	T0,T8	0	High-speed Data Memory Inputs. (MD0-MD7)
	U6, 24	$\overline{\text{I/O A1}}$	T1,T9	1	
	U6, 25	$\overline{\text{I/O A2}}$	T2,T10	2	
	U6, 30	$\overline{\text{I/O A3}}$	I3,T11	3	
	U6, 31	$\overline{\text{I/O A4}}$	T4,T12	4	
	U6, 36	$\overline{\text{I/O A5}}$	T5,T13	5	
	U6, 37	$\overline{\text{I/O A6}}$	T6,T14	6	
	U6, 2	$\overline{\text{I/O A7}}$	T7,T15	7	
9	U6,20	$\overline{\text{I/O B0}}$	MA5	0	Data Memory Address Count
	U6, 23	$\overline{\text{I/O B1}}$	MA4	1	
	U6, 26	$\overline{\text{I/O B2}}$	MA3	2	
	U6, 29	$\overline{\text{I/O B3}}$	MA2	3	
	U6, 32	$\overline{\text{I/O B4}}$	MA1	4	
	U6, 35	$\overline{\text{I/O B5}}$	MA0	5	
	U6, 38	$\overline{\text{I/O B6}}$	HMF	6	High=Memory Full.
	U6, 1	$\overline{\text{I/O B7}}$	HTP	7	High=Trigger Present.

Table 8-4. Examples of Observed Error Messages and Related Failures

First Error and Diagnostic Displayed					Other Error Codes	Cause
P1	Code	P4	P3	P2		
8F	E60			5	none	A1U14
80	E61				E71-77, 85	A1U14
10	E62			3	E70-91	A1U35 or U36
40	E62			3	E65, 70-91	A1U24
80	E62			3	none	A1U14 pin 1 short to ground
FF	E62			3	E65, 70-91	A1U14
2	E63			2	none	A3U23 (display)
20	E67			E5	E70-91	A1U11, U12, or U16
0F	E70	30	50	50	E71-86	A1U13A
1F	E70	20	20	20	E71-86	A1U13A
3b	E70	00	40	40	E71-91	A1U7 or U16
3d	E70	00	02	02	E71-86, 88	A1U45
3E	E70	00	01	01	E71-91	A1TP2 short to gnd.
3F	E70	00	00	XX	E71-91	A1U16
3F	E70		0F	00	E71-85	A1U1
3F	E70	C0	00	00	E71-91	A1Q2, U15, U19, U22, U24, or U26
3F	E70	C0	00	EF	E72-91	A1Q2
3F	E70	C0	00	FF	E72-91	A1Q1
3F	E70	1F	00	00	E72-77, 79-91	A1U43
3b	E71	00	08	00	E72-77, 79-91	A1U7
3F	E71	00	01	00	E72-77, 80, 81, 85-91	A1U2
3F	E71	00	0F	0F	E72-77, 79-91	A1U17D short to gnd.
3F	E71	00	7E	7E	E72-77, 79-91	A1U19
3F	E71	00	db	db	E72-77, 79-91	A1U17D
3F	E71	00	E0	E0	E72-91	A1U20
3F	E71	00	E3	E3	E72-77, 79-91	A1U28
3F	E71	00	F1	F1	E72, 73, 75-77, 79, 80, 82-84, 87-91	A1U40
3F	E71	24	3F	3F	E72-77, 85	A1U42E
3F	E71	41	AA	AA	E72-77, 85	A1U20A
3F	E73	C0	65	65	E80, 85, 87, 91	A1U1 (heat)
3F	E74	C0	67	67	E81, 84-86, 90	A1U37
3F	E80	00	1F	1F	E81-85	A1U28

Table 8-5. 1602A Mnemonics

MNEMONIC	DESCRIPTION
a-g	Display (seven-segment LED) anode control lines. High level causes segment to light.
A1-A5	Address switch lines 1-5. Low level indicates corresponding section of HP-IB Address switch is in the "1" position.
ACDS	Accept Data State. Allows 1602A Acceptor Handshake function to prevent an input byte (on bus DIO lines) from being removed until the 1602A has had enough time to capture the byte.
ACK	Acknowledge. When high, 1602A has talk data-byte ready for bus transmission. After transmitted data-byte has been accepted by listener(s), ACK is sent low.

Table 8-5. 1602A Mnemonics (Cont'd)

MNEMONIC	DESCRIPTION
ATN	Attention. When low, bus Controller is sending commands that designate listener(s) and talker (Command Mode). When high, designated talker transmits to designated listener(s) (Data Mode).
B0-B15	Bit 0-15. Input data bits from system under test.
C1-C4	Column lines 1-4. Tied to keyboard matrix columns. A low-going pulse on one of these lines tells the μP that "a key is down, and it is in this column."
DAV	Data Valid. When low, talker is signalling to listeners that data on DIO bus lines is valid.
DI01-DI08	Data Input/Output lines. Bidirectional HP-IB signal lines that carry message bytes between instruments in bit-parallel byte-serial form.
EOI	End or Identify. This bus function not used by 1602A.
HAL	High, Addressed to Listen. True when 1602A has received its listen address from the Controller (bus in Command Mode). When true, allows 1602A to receive its device-dependent commands (listen) during bus Data Mode operation (enables Acceptor Handshake).
HAT	High, Addressed to Talk. True when 1602A has received its talk address from the Controller (bus in Command Mode). When true, allows 1602A to transmit its measurement status or results (talk) during bus Data Mode operation (enables Source Handshake).
HATN	High, Attention. True when bus in Command Mode (ATN = low). Enables Acceptor Handshake during bus Command Mode operation. Complement of LATN.
HCT	High, Clear Test. True when clock and clock qualifier present tests are reset. When true, Clock Present Latch (A1U24A) and Clock Qualifier Present Latch (A1U28A) are cleared.
HCTA	High, Clear Trigger Address Counters. When true, Trigger Address Counters/Data Latches A1U4, U9, U11, U12 are cleared in preparation for data acquisition.
HCLP	High, Clock Present. When true, Clock Present Latch (A1U24A) is reporting the presence of a clock pulse to the μP. If not again true within approximately 300ms after reset by HCT, message E42 is displayed.
HDACD	High, Data Accept Drive. When true, sends 1602A NDAC bus output high. This signals that 1602A has accepted an input byte from DIO lines.
HDAVD	High, Data Valid Drive. Complement of LDAVD. When true, enables A4U1C (to clear ACK flip-flop A4U2A as soon as listener(s) have accepted the 1602A output data byte).
HITA	High, Enable Trigger Address Counter Increment. When true, Trigger Address Counters/Data Latches A1U4, U9, U11, U12 are placed in their count mode.
HKYD	High, Key Down. True after μP finds a pressed key. When true, prevents multiple entries. Returned low after all keys read in the up position for one scan cycle.
HKYSTR	High, Key Strobe. True when μP is interrogating a keyboard matrix row. When true, causes a current ramp that drives key switches in the row.
HLA	High, Listen Address. When true, Controller is sending a listen address (bus in Command Mode). Bus DIO inputs must match 1602A Address switch positions in order for the 1602A to become a listener in Data Mode.
HLT	High, Load Trigger. When true, μP sets Clock Switch A1U19, U26 to LOAD TRIG clock.
HMA	High, My Address. True when bus DIO inputs (LD0-LD4) match 1602A Address switch lines (A1-A5).
HMF	High, Memory Full. True when Data Memory A1U7, U16 has captured the desired 64 words from the system under test.
HMLA	High, My Listen Address. True when Controller is sending a listen address that matches 1602A bus address (bus in Command Mode).
HMTA	High, My Talk Address. True when Controller is sending a talk address that matches 1602A bus address (bus in Command Mode).
HOTA	High, Other Talk Address. True when Controller is sending a talk address that doesn't match 1602A bus address (bus in Command Mode).
HPCLS	High, Positive Clock Slope. True when μP indicates that positive edge external clock was selected to strobe data into the 1602A. When false, negative edge selected.
HPLOG	High, Positive Logic. True when μP indicates positive logic polarity selected.
HQLP	High, Clock Qualifier Present. When true, Clock Qualifier Present Latch (A1U28A) is reporting the presence of a qualified clock to the μP. If not again true within approximately 300ms after reset by HCT, message E41 displayed.

Table 8-5. 1602A Mnemonics (Cont'd)

MNEMONIC	DESCRIPTION
HRDY	High, Ready. When true, 1602A is enabled to signal the bus that it is "ready for data."
HREN	High, REN. True when bus REN (Remote Enable) input is low.
HRFD	High, Ready For Data. When true, sends 1602A NRFD bus output high. This signals that 1602A is ready to accept an input byte from DIO lines.
HRTE	High, Record Trigger Events. True when μP indicates that TRACE EVENTS mode was commanded. When true, only events that satisfy trigger plus delay specification are captured by the Data Memory A1U7, U16.
HRTL	High, Return To Local. Momentarily true when RETURN TO LOCAL key is pressed. When true, allows keyboard to resume control unless Controller has previously sent a Local Lock Out Command.
HSTART	High, Start. True when Trigger plus Delay STARTS Trace is selected. Complement of LSTART.
HSTOP	High, Stop. True when Trace is completed, or stopped by STOP key. When true, A1U8C is enabled (to extinguish TRACE indicator on display).
HSTRB	High, Strobe. True for approximately one PDSPCK cycle at the start of a display cycle. When true, causes the beginning of the display LED strobing sequence.
HTF	High, Trigger Found. True when A1U22B detects a qualified trigger pattern.
HTA	High, Talk Address. When true, Controller is sending a talk address (bus in Command Mode). Bus DIO inputs must match 1602A Address switch positions in order for the 1602A to become the talker in Data Mode.
HTP	High, Trigger Present. True when trigger plus delay condition is detected during a Trace.
HUN	High, Unlisten Enable. True when bus DIO inputs 1 thru 5 are low. Used with HLA to detect universal unlisten command from Controller (bus in Command Mode).
HUNL	High, Unlisten. True when bus Controller sends universal unlisten command (HUN and HLA true). When true, 1602A unaddresses itself as a listener.
HWE	High, Write Enable. When true, A1U8A is enabled (to produce a write enable pulse for Data Memory A1U7, U16). When set low, the negative edge causes Data Memory Address Counters A1U1, U5 to be incremented via A1U3A.
IFC	Interface Clear. When set low by bus Controller, this input causes 1602A to clear its talk and listen functions.
LAHEN	Low, Acceptor Handshake Enable. True when bus in Command Mode or 1602A addressed to listen in Data Mode. When true, 1602A allowed to participate in bus handshakes as an acceptor (control NDAC and NRFD).
LATN	Low, Attention. True when bus ATN input is low (Command Mode).
LB0-LB7	Low, Bits 0-7. 1602A output data to bus DIO lines (HP-IB is low = true); or "latched" input data from bus DIO lines.
LD0-LD7	Low, Data 0-7. 1602A input data from bus DIO lines (HP-IB is low = true).
LDAVD	Low, Data Valid Drive. True when 1602A is transmitting a bus data byte (LB0-LB7). When true, 1602A sets bus DAV output low to signal valid data to listener(s).
LDBE	Low, Delay By Events. When true, Trigger Recognition RAM Comparators A1U2, U23 remain enabled. Delay Generator A1U37-U40 may only be incremented when RAM Comparators report that trigger pattern is present.
LGTL	Low, Go To Local. True when bus Controller sends Go To Local message (LD2, LD5, LD6 = high; LD1 = high; LD3, LD4 = high; LD0 = low) in Command Mode. When true, and 1602A addressed to listen, keyboard is allowed to resume control.
LINIT	Low, Initialize. True when IFC or LPON low. When true, causes 1602A to initialize to both untalk and unlisten configuration for bus operation.
LL9	Low, Load 9. True at the start of a key scan cycle. When true, A2U1 presets to a count of 9 for a known starting point when keyboard is scanned.
LL0	Low, Establish Local Lock Out. True when bus Controller sends Local Lock Out message (LD2, LD5, LD6 = high; LD1 = high; LD4 = low; LD3 = high; LD0 = low) in Command Mode. When true, A4U3C output causes 1602A to ignore RETURN TO LOCAL key. Local operation (keyboard control) may be resumed only when Controller: commands Go To Local (LGTL), or sets REN high.
LO	Low, Local Locked Out. True when A4U3C responds to bus LLO command.
LPCLS	Low, Positive Clock Slope. Complement of HPCLS.
LPCQP	Low, Probe Clock Qualifier Present. True when Data Probe CLOCK QUAL input is high.

Table 8-5. 1602A Mnemonics (Cont'd)

MNEMONIC	DESCRIPTION
LPON	Low, Power On. Momentarily low when power is applied to 1602A to set initial conditions for HP-IB operation.
LPRB	Low, Processor Reading Buffer. When true, 1602A is reading its input data buffer to determine the device-dependent command (bus in Data Mode).
LREM	Low, Remote. Set low when bus REN input is low and 1602A receives its listen address. When true, 1602A is enabled to receive its device-dependent commands. Also, keyboard ignored except RETURN TO LOCAL key.
LREST	Low, Reset. True when μP reports a Trace command. When true, causes: Data Memory Address Counters A1U1 and U5 to be cleared, Trigger Present flag to be cancelled, and TRACE POINT OUT to be set low.
LSHEN	Low, Source Handshake Enable. True when bus in Data Mode and 1602A addressed to talk. When true, 1602A enabled to drive DAV and to output data bytes on DIO lines.
LST	Low, Self-Test. True when 1602A conducting its internal self-test at power on.
LSTOP	Low, Stop. When true, causes TRACE indicator on display to be extinguished.
LSTART	Low, Start. True when Trigger plus Delay STARTS Trace is selected. False when Trigger plus Delay ENDS Trace is selected.
LTON	Low, Talk Only. True when 1602A ADDRESSABLE/TALK ONLY switch set to TALK ONLY.
LWE	Low, Write Enable. When true, latched data from system under test is loaded into data Memory A1U7, U16. Address written to is determined by output of Data Memory Address Counters A1U1, U5.
MA0-MA5	Memory Address lines for Data Memory A1U7, U16.
MD0-MD7	Memory Data lines. Output data from Data Memory.
NDAC	Data Not Accepted. When high, all bus listeners are signalling acceptance of a DIO lines data byte.
NDSPCK	Negative, Display Clock. Complement of PDSPCK and HKYSTR.
NIMA	Negative, Increment Memory Address. Negative edge causes Data Memory Address Counters A1U1, U5 to be clocked. The μP drives this signal to access the Data Memory word desired for display.
NRFD	Not Ready For Data. When high, all bus listeners are signalling that they are ready for a data byte to be placed on DIO lines.
PACKCK	Positive, ACK Clock. Positive edge clocks ACK flip-flop A4U2A.
PCLK	Probe Clock. Clock from system under test sent to 1602A via Data Probe.
PDCK	Positive, Data Latch Clock. Positive edge clocks Trigger Address Counters/Data Latches A1U4, U9, U11, U12 according to output of Clock Switch A1U19.
PDRC	Positive, Delay Control Register Clock. Positive edges clock new delay value into Delay Control Registers A1U35, U36 (via TML line) each time Delay specification is changed.
PDSPCK	Positive, Display Clock. Positive edges clock Display Cathode Drivers to strobe LEDs. Also clocks A2U1 for keyboard row scanning.
PDYCK	Positive, Delay Clock. Positive edges clock: Delay Generator A1U37-U40, Trigger Latches A1U29A, U29B, and Clock Qualifier Present Latch A1U28A. Complement of HWE.
PITA	Positive, Increment Trigger Address. Positive edges cause Trigger Address Counters/Data Latches A1U4, U9, U11, U12 to be incremented when μP is loading trigger pattern into RAM Comparators A1U2, U23.
PQCK	Positive, Qualifiers Present Clock. Positive edges clock: Clock Present Latch A1U24A, A1U25A to determine if Trigger Qualifier is present, and A1U25B to determine if Clock Qualifier is present.
PRNR	Positive, Release Not Ready. Positive edge from μP allows 1602A to resume participation in bus handshakes.
REN	Remote Enable. When low, 1602A is enabled to go to remote operation (if also addressed to listen) in order to receive its device-dependent bus commands.
SRQ	Service Request. This bus Function not used by 1602A.
$\overline{T0}$-$\overline{T15}$	Latched input data bits from Data Probe. Applied to RAM Comparators A1U2, U23 (for trigger recognition) and to Data Memory A1U7, U16.
TML	Lower Trigger Memory Input Data Line. Used to load trigger data into RAM Comparator A1U2. Also used to load delay value into Delay Control Registers A1U35, U36 and to enable Data Memory chip A1U16.
TMU	Upper Trigger Memory Input Data Line. Used to load trigger data into RAM Comparator A1U23. Also used to enable Data Memory chip A1U7.

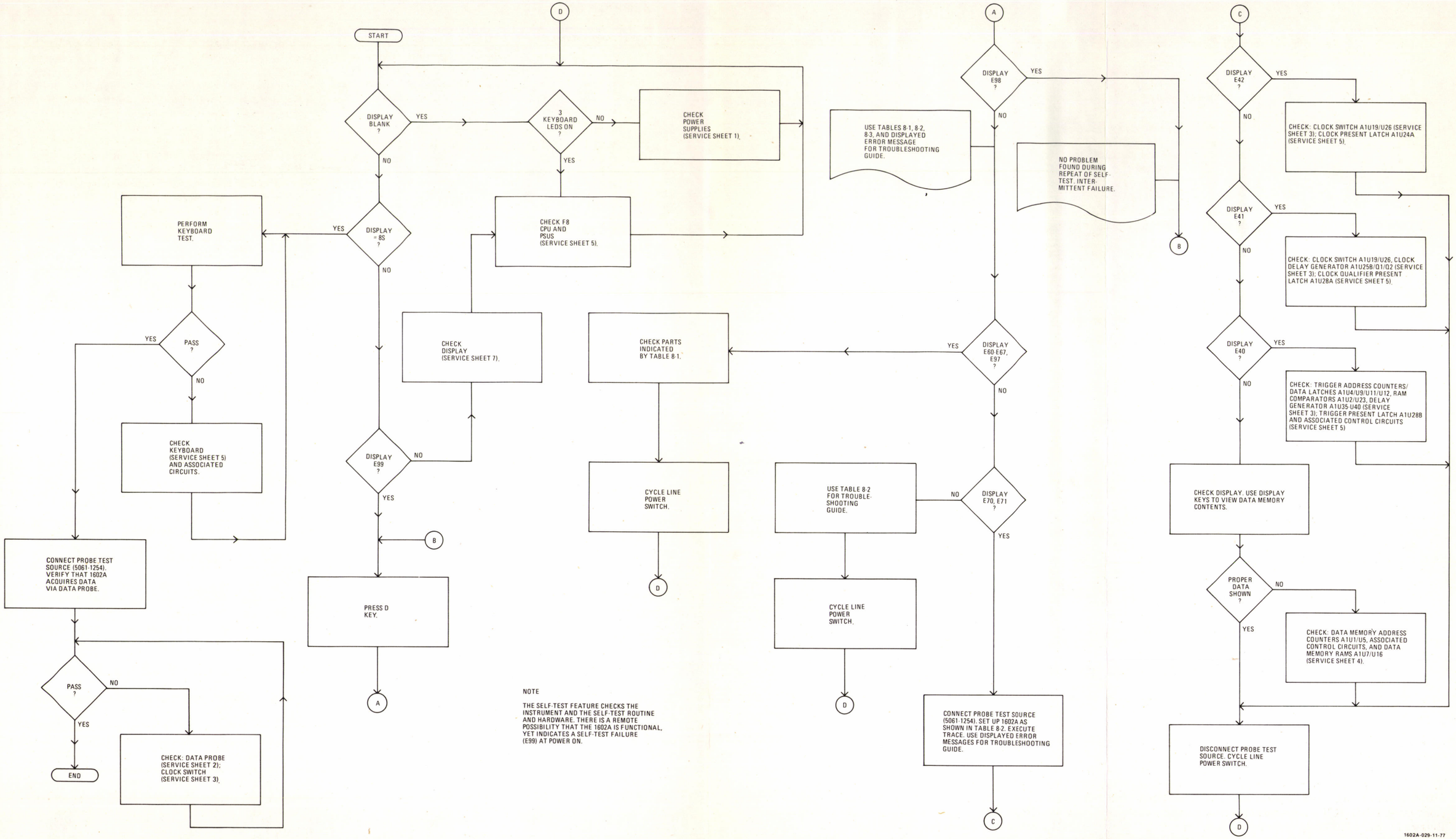


Figure 8-2.
Troubleshooting Flow Chart

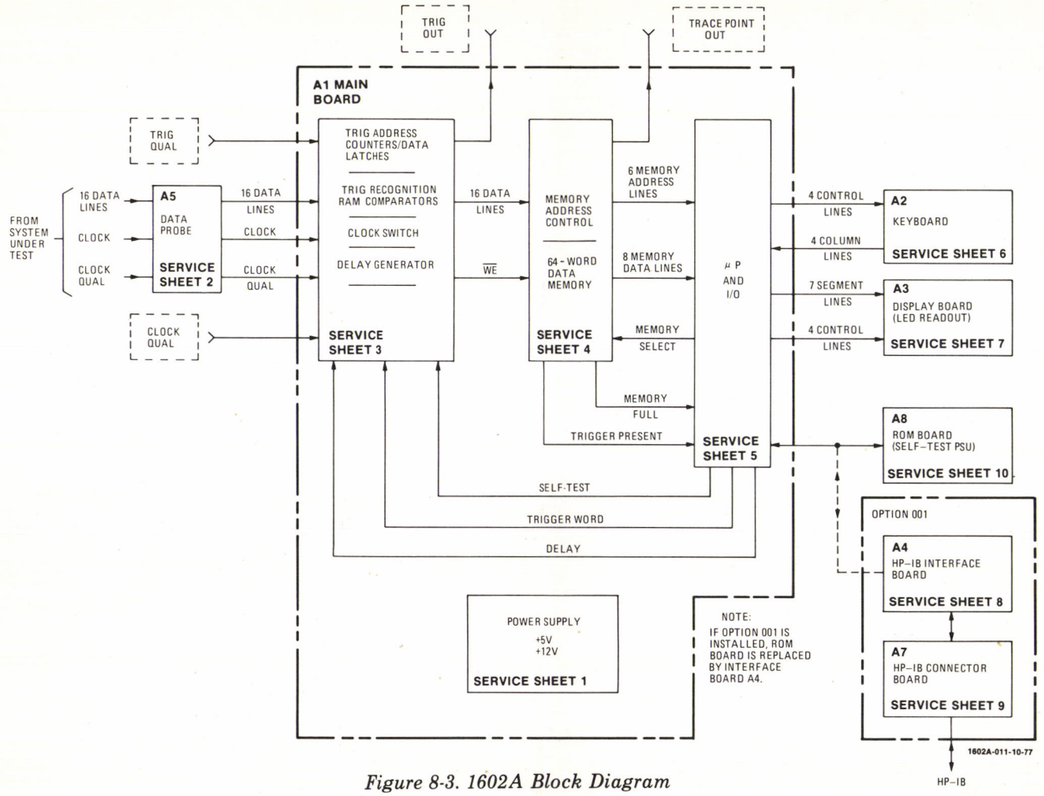


Figure 8-3. 1602A Block Diagram

BLOCK DIAGRAM DESCRIPTION

The 1602A is controlled by an F8 microprocessor (μP) and program storage units (PSUs) which:

a. Conduct self-test when 1602A is powered on.
b. Read the Keyboard to determine Format and Trace Specification.
c. Load Trigger Word into RAM Comparators.
d. Load Delay value into Delay Generator and command delay by Clocks or Events.
e. Select clock.
f. Command Trace mode (Starts, Ends, or Events).
g. Control display of acquired data.

Data from the system under test is applied to the Data Probe and strobed into the Data Latches by clock pulses from the system under test. When a Trigger Word is recognized the Delay Generator is incremented until the delay (either Clocks or Events) is counted out.

TRIG OUT goes high when Trigger plus Delay is satisfied and returns low approximately one external clock later. TRIG OUT is enabled as soon as Trigger and Delay are entered (a TRACE command is not required).

The 64 word Data Memory (16 bits wide) is controlled by a high-speed memory controller during data acquisition. The memory controller receives commands from the μP that cause it to work in one of three modes; (1) Trigger plus Delay STARTS Trace, (2) Trigger plus Delay ENDS Trace, or (3) Trace EVENTS.

The Data Memory is controlled by the μP during the display cycle. When both Trigger Present and Memory Full are reported to the μP, the data acquisition cycle is completed. The μP accesses the word desired for display by incrementing the Data Memory address counter.

TRACE POINT OUT goes low when TRACE key is pressed and returns high when the Trigger plus Delay event occurs that starts or ends the Trace (in STARTS or ENDS mode respectively).

The μP formats data from the Data Memory and causes it to be displayed by seven-segment LEDs on the Display Board.

With Option 001 installed, the 1602A can receive commands via HP-IB that simulate front-panel key entries. The 1602A assumes a measurement configuration, executes the measurement, and configures to transmit measurement status or results to other HP-IB instruments.

SERVICE SHEET 1

PRINCIPLES OF OPERATION

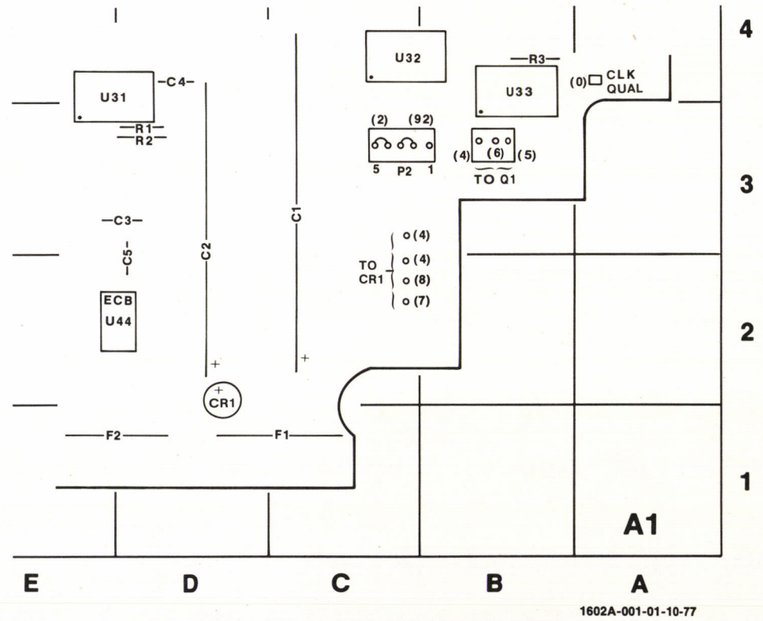
The power supply operates from 100, 120, 200, or 240 VAC line voltages. Refer to LINE VOLTAGE SELECTION in Section II to set the 1602A AC Line Selector for proper operation. The supply provides regulated +5 V and +12 V to the 1602A.

Front-panel switch S1 applies line voltage to transformer T1 primary. T1 is protected by line fuse F1 (located in the read panel AC power module). T1 secondaries are rectified by bridge rectifiers A1CR1 and CR1 (CR1 mounted on inside rear panel).

+12 V POWER SUPPLY. A1CR1 output is filtered by C2 and C5. This output is applied to voltage regulator U44. U44 output is filtered by C3. U44 provides Vcc for U31 and +12 V for the 1602A. Fuse A1F2 protects the +12 V supply.

+5 V POWER SUPPLY. CR1 output is filtered by C1 and applied to Darlington pair Q1 (mounted on inside rear panel). Q1 regulates the +5 V supply. U31 controls Q1 conduction. U31 reference voltage output is divided by R1 and R2 and applied to U31 noninverting input. Q1 emitter (+5 V output) is applied to U31 inverting input. If the supply output falls below +5 V, then U31 Vout voltage increases. This causes Q1 to conduct harder, and its emitter voltage (+5 V output) increases because Vce decreases. If the supply voltage tries to increase to more than +5 V, then U31 Vout decreases, Q1 conducts less, and the output voltage decreases. The +5 V supply will not work if +12 V (U31 Vcc) is not present. Fuse A1F1 protects the +5 V supply.

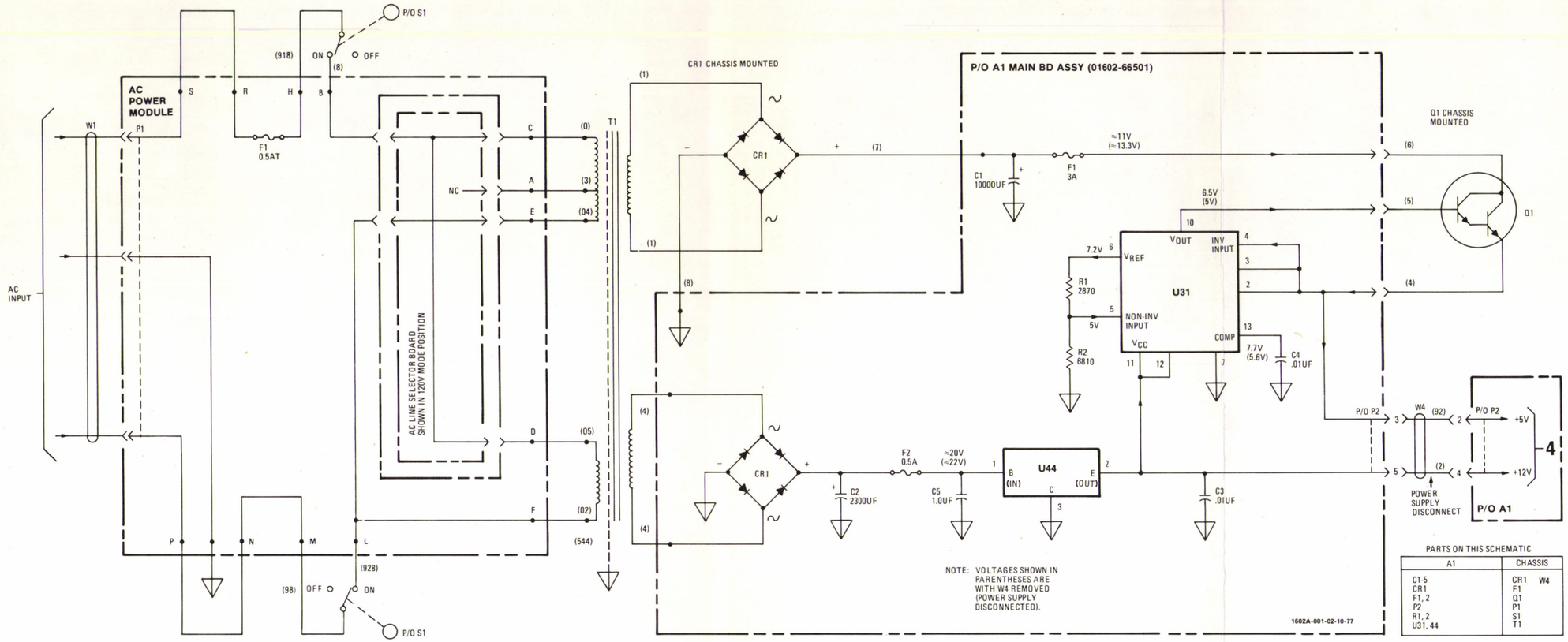
Molex cable W4 allows power supplies to be quickly disconnected from the 1602A. This provides isolation when troubleshooting is required.



Power Supply P/O A1 Component Locator
(01602-66501)

REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	C-3	P2	C-3
C2	D-3	R1	D-3
C3	D-3	R2	D-3
C4	D-4	R3	B-4
C5	D-2	U31	E-4
CR1	D-2	U32	C-4
F1	C-1	U33	B-4
F2	D-1	U44	D-2

Figure 8-4. Service Sheet 1, Power Supply (Sheet 1 of 2)



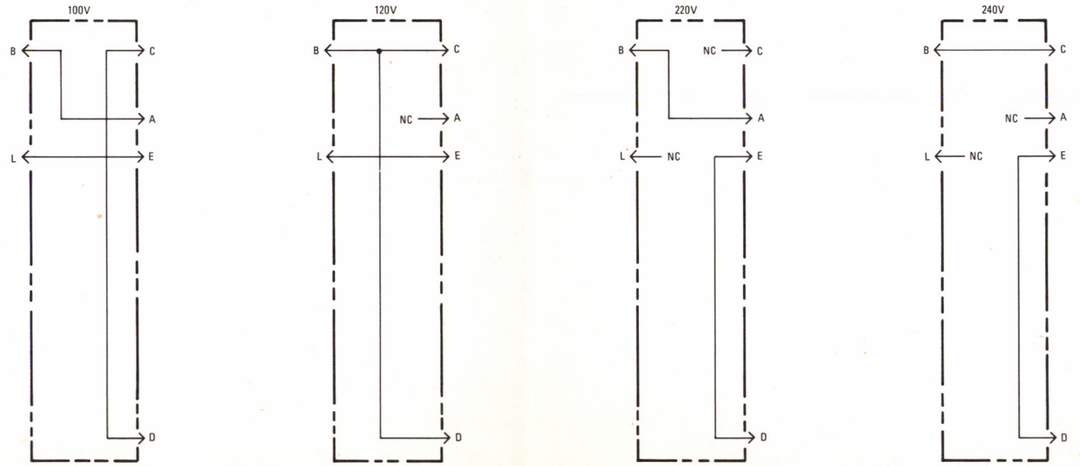
PARTS ON THIS SCHEMATIC

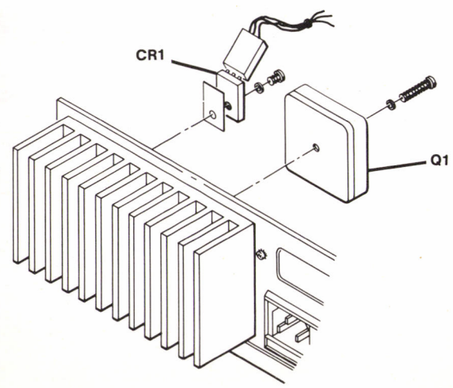
A1	CHASSIS
C1-5	CR1 W4
CR1	F1
F1, 2	Q1
P2	P1
R1, 2	S1
U31, 44	T1

ACTIVE DEVICES ON THIS SCHEMATIC

REF DES	HP PART NO.	MFR. PART NO.
CR1	1906-0093	MDA3501
Q1	1854-0558	1854-0558
A1CR1	1906-0006	1906-0006
A1U31	1826-0409	UA723DM
A1U44	1826-0147	7812UC

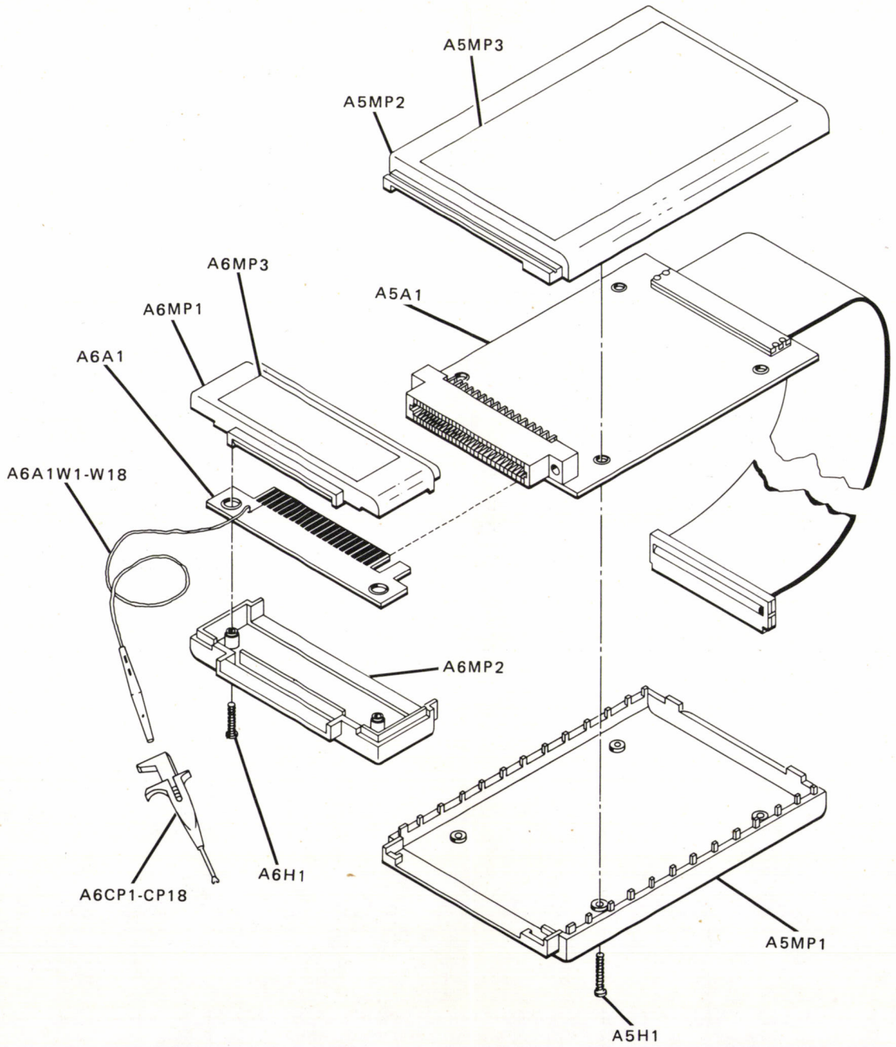
AC LINE SELECTOR BOARD MODES (WIRING DIAGRAMS)



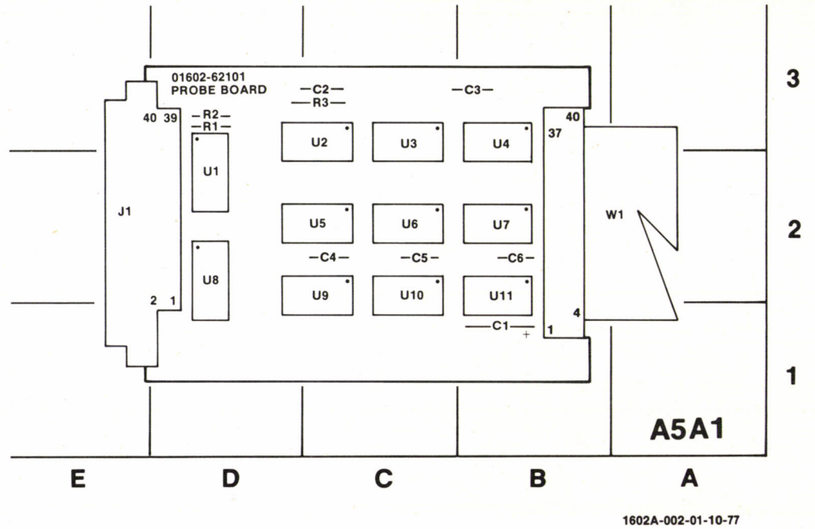


1

Figure 8-4. Service Sheet 1, Power Supply (Sheet 2 of 2)



Probe Assembly A5 and Probe Interface Wire - Adapter Assembly A6 Parts Breakdown



Probe Board A5A1 Component Locator
(01602-66501)

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	B-1	R1	D-3	U5	C-2
C2	C-3	R2	D-3	U6	C-2
C3	B-3	R3	C-3	U7	B-2
C4	C-2	U1	D-2	U8	D-2
C5	C-2	U2	C-3	U9	C-2
C6	B-2	U3	C-3	U10	C-2
J1	E-2	U4	B-3	U11	B-2
				W1	A-2

Figure 8-5. Service Sheet 2, Data Probe A5A1 (Sheet 1 of 2)

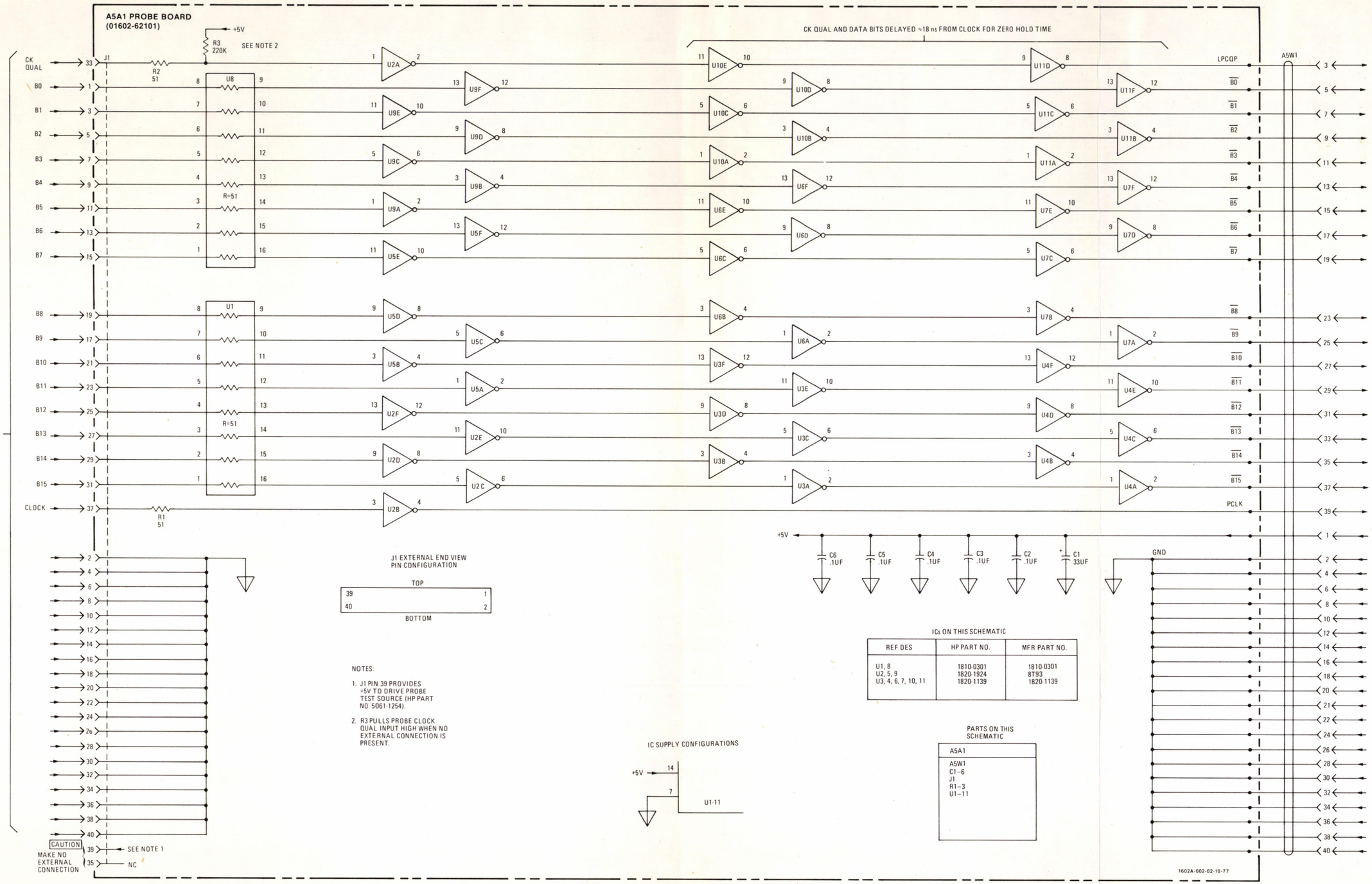


Figure 8-5. Service Sheet 2, Data Probe A5A1 (Sheet 2 of 2)

SERVICE SHEET 3

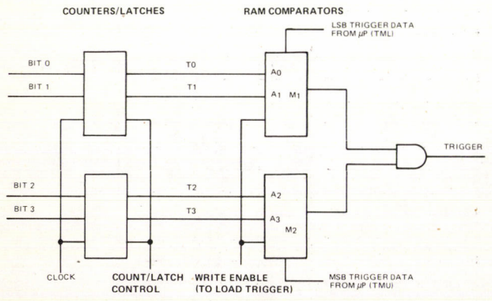
PRINCIPLES OF OPERATION

TRIGGERING. Pattern recognition triggering is done with two, 256 x 1-bit RAM comparators (U2, U23). The μP (microprocessor) loads the desired trigger pattern into U2 and U23. Incoming data is then compared to this pattern. When a match occurs, the RAM comparator output goes high. U2 and U23 outputs are ANDed together to provide 16-bit trigger capability. When both RAMs output a match simultaneously, a trigger pulse (HI = Trigger Found) is produced (U22B).

The μP loads U2 and U23 with the trigger pattern by configuring Trigger Address Counters/Data Latches (U4, U9, U11, U12) into their count mode. The μP then writes the desired bit condition (1 or 0) via TML or TMU lines to the RAM address indicated by counter output. The counters are then incremented to provide the next RAM address.

The Counters/Latches are placed in their latch mode (μP sends parallel enable inputs low) after U2 and U23 are loaded. Data from Data Probe A5 (Service Sheet 2) is latched by the selected external clock edge (from system under test). The latched data is applied to the RAM comparators for trigger recognition and to the 64-word Data Memory (Service Sheet 4).

The concept of this triggering method is shown by a four-bit pattern trigger circuit. If the desired trigger pattern is $\left\{\begin{matrix}\text{Bit 3} & \text{Bit 2} & \text{Bit 1} & \text{Bit 0}\\ 1 & 0 & 1 & 1\end{matrix}\right\}$ then the RAM comparators should be loaded with a match (1) or a no match (0) at addresses $\left\{\begin{matrix}A_3 & A_2 & A_1 & A_0\\ 1 & 0 & 1 & 1\end{matrix}\right\}$ for trigger recognition.



Four-Bit Pattern Trigger Circuit

CLOCK SWITCH (U19, U26). Allows the μP to choose between: (a) positive edge external clock, (b) negative edge external clock, (c) load trigger clock, or (d) self-test clock (2 MHz). During the transmission of a trigger or delay word, or at the beginning of a Trace, the Clock Switch is set to load trigger clock. This prevents the 1602A from accepting data until it is internally set up for the measurement.

DELAY. Once the desired trigger pattern has been found, delay by Clocks or Events is enabled. In delay by Clocks mode (LDBE = high), the chip select lines of RAM comparators U2 and U23 are set high by U29A $\overline{Q}$ output. This disables further pattern recognition and preserves U22B output high. The Delay Generator (U37-U40) is then incremented by each qualified external clock (from Clock Delay Generator) when delay is set to greater than zero.

In delay by Events mode (LDBE = low), U2 and U23 remain enabled (chip select lines set low by U29A $\overline{Q}$). This allows the Delay Generator to be incremented only when the trigger pattern is present.

When the delay is counted out, the Delay Generator is reloaded from the Delay Control Register (U35, U36). Also, U2 and U23 chip select lines are reset low to enable pattern recognition.

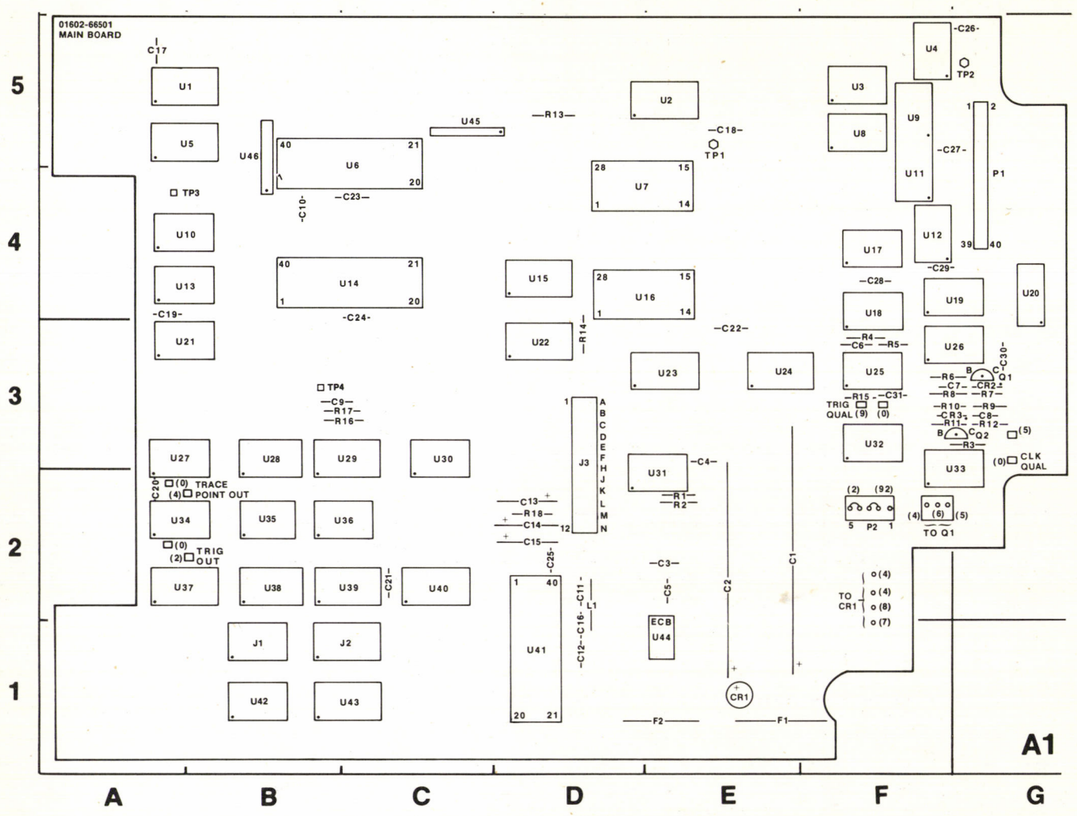
The Delay Control Register is a serial-in-parallel-out register that is loaded (via TML and PDRC lines) from the μP whenever the delay number is changed. At the end of the delay word transmission cycle, the μP stops the Delay Generator (U22D output goes low) and parallel loads it with the 1's complement of the new delay value.

CLOCK QUALIFIERS. The 1602A has two CLOCK QUAL inputs. One is a rear-panel BNC input and the other is a Data Probe input. They both provide the same function, although set-up and hold time specifications differ. Both are pulled high when disconnected. When high, the 1602A is qualified, allowing data to be clocked into memory by the external clock. When low, trigger recognition, delay, and memory loading are inhibited (HWE and PDCK disabled).

When Probe CLOCK QUAL input is high, LPCQP (low, Probe Clock Qualifier Present) is true.

TRIGGER QUALIFIER. The rear-panel TRIG QUAL input provides an additional Trace Point Qualifier in parallel with the 16 data lines from Data Probe A5. When low, trigger words are not recognized. TRIG QUAL is pulled high (by R15) when disconnected. When high, U25A causes U8B output to be high.

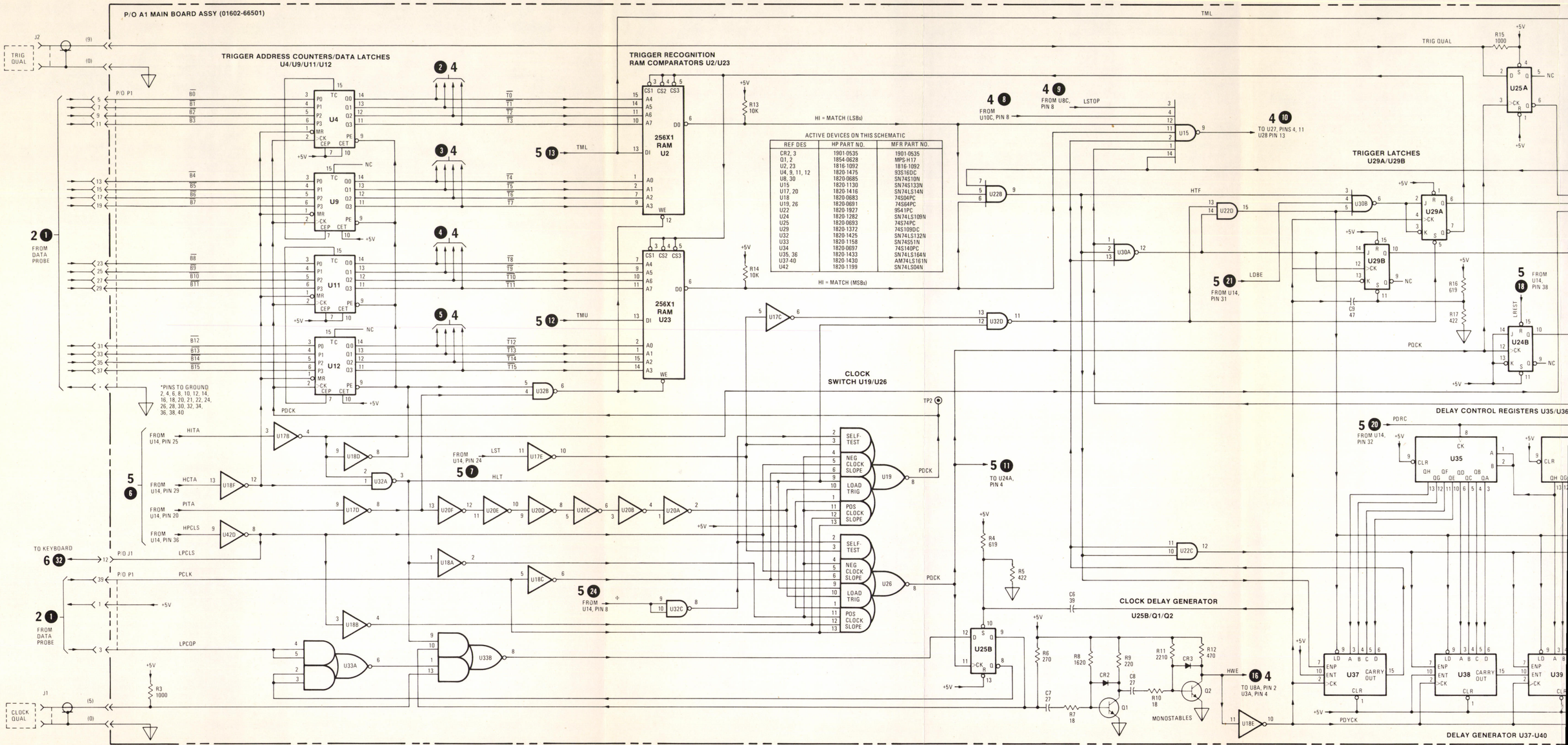
TRIGGER OUTPUT. Each time trigger plus delay condition is detected U29B causes TRIG OUT to go high. Approximately one external clock later, TRIG OUT returns low. TRIG OUT pulses are produced whether or not the 1602A is performing a Trace.



Main Board A1 Component Locator
(01602-66501)

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	E-2	C15	D-2	C29	F-4	Q1	G-3	R13	D-5	U5	A-5	U19	G-4	U33	G-2
C2	E-2	C16	D-1	C30	G-3	Q2	G-3	R14	D-3	U6	C-5	U20	G-4	U34	A-2
C3	E-2	C17	A-5	C31	F-3	R1	E-2	R15	F-3	U7	D-4	U21	A-3	U35	B-2
C4	E-3	C18	E-5	CR1	E-1	R2	E-2	R16	C-3	U8	F-5	U22	D-3	U36	C-2
C5	E-2	C19	A-4	CR2	G-3	R3	G-3	R17	C-3	U9	F-5	U23	E-3	U37	A-2
C6	F-3	C20	A-2	CR3	F-3	R4	F-3	R18	D-2	U10	A-4	U24	E-3	U38	B-2
C7	G-3	C21	C-2	F1	E-1	R5	F-3	TP1	E-5	U11	F-4	U25	F-3	U39	C-2
C8	G-3	C22	E-3	F2	E-1	R6	F-3	TP2	G-5	U12	F-4	U26	G-3	U40	C-2
C9	B-3	C23	C-4	J1	B-1	R7	G-3	TP3	A-4	U13	A-4	U27	A-3	U41	D-1
C10	B-4	C24	C-4	J2	C-1	R8	F-3	TP4	B-3	U14	C-4	U28	B-3	U42	B-1
C11	D-2	C25	D-2	J3	D-3	R9	G-3	U1	A-5	U15	D-4	U29	C-3	U43	C-1
C12	D-1	C26	G-5	L1	D-2	R10	F-3	U2	E-5	U16	E-4	U30	C-3	U44	E-1
C13	D-2	C27	G-5	P1	G-4	R11	F-3	U3	F-5	U17	F-4	U31	E-2	U45	C-5
C14	D-2	C28	F-4	P2	F-2	R12	G-3	U4	F-5	U18	F-4	U32	F-3	U46	B-5

Figure 8-6. Service Sheet 3, Data Registration, Trigger Recognition, and Delay (Sheet 1 of 2)


P/O A1 MAIN BOARD ASSY (01602-66501)
TRIGGER ADDRESS COUNTERS/DATA LATCHES U4/U9/U11/U12
TRIGGER RECOGNITION RAM COMPARATORS U2/U23
256X1 RAM U2
256X1 RAM U23
ACTIVE DEVICES ON THIS SCHEMATIC
REF DES | HP PART NO. | MFR PART NO.
CR2, 3 | 1901-0535 | 1901-0535
Q1, 2 | 1854-0628 | MPS-H17
U2, 23 | 1816-1092 | 1816-1092
U4, 9, 11, 12 | 1820-1475 | 93S16DC
U8, 30 | 1820-0685 | SN74S10N
U15 | 1820-1130 | SN74S133N
U17, 20 | 1820-1416 | SN74LS14N
U18 | 1820-0683 | 74S04PC
U19, 26 | 1820-0691 | 74S64PC
U22 | 1820-1927 | 9S41PC
U24 | 1820-1282 | SN74LS109N
U25 | 1820-0693 | 74S74PC
U29 | 1820-1372 | 74S109DC
U32 | 1820-1425 | SN74LS132N
U33 | 1820-1158 | SN74S51N
U34 | 1820-0697 | 74S140PC
U35, 36 | 1820-1433 | SN74LS164N
U37-40 | 1820-1430 | AM74LS161N
U42 | 1820-1199 | SN74LS04N
HI = MATCH (LSBs)
HI = MATCH (MSBs)
TRIGGER LATCHES U29A/U29B
CLOCK SWITCH U19/U26
CLOCK DELAY GENERATOR U25B/Q1/Q2
MONOSTABLES
DELAY CONTROL REGISTERS U35/U36
DELAY GENERATOR U37-U40
*PINS TO GROUND 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 21, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40
TRIG QUAL
CLOCK QUAL
TML
TMU
TMLE
PDCK
PDYCK
HWE
HTF
LOBE
LSTOP
HITA
HCTA
PITA
HPCLS
LPCLS
PCLK
LPCOP
TO KEYBOARD
FROM DATA PROBE
TO U8A, PIN 2 U3A, PIN 4
TO U24A, PIN 4
TO U27, PINS 4, 11 U28 PIN 13
FROM U8C, PIN 8
FROM U10C, PIN 8
FROM U14, PIN 38
FROM U14, PIN 32
FROM U14, PIN 31
FROM U14, PIN 24
FROM U14, PIN 8
FROM U14, PIN 25
FROM U14, PIN 29
FROM U14, PIN 20
FROM U14, PIN 36

Data Reco

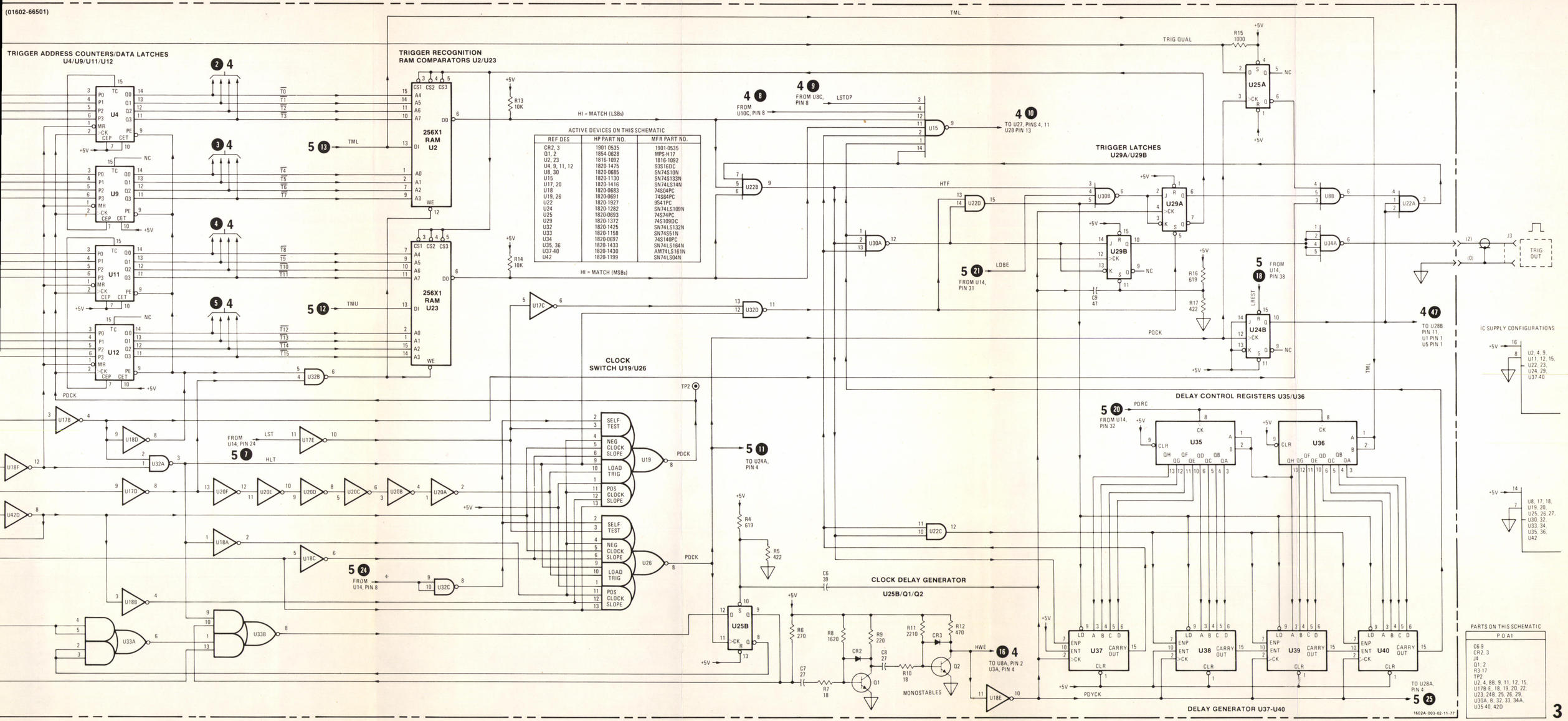


Figure 8-6. Service Sheet 3, Data Recognition, Trigger Recognition, and Delay (Sheet 2 of 2)

SERVICE SHEET 4

PRINCIPLES OF OPERATION

The 16-bit x 64-word Data Memory (U7, U16) stores data from the system under test during the data acquisition cycle. When the measurement is completed (or stopped), this acquired data is sent to the display (via the μP) for viewing by the operator.

The Data Memory is controlled by a high-speed memory controller during data acquisition. During the display cycle the Data Memory is controlled by the μP.

The memory controller is made up of Data Memory Address Counters (U1, U5), their associated control circuitry, and a write enable control (U8A).

The memory controller works in one of three modes as commanded by the μP: (1) trigger plus delay STARTS Trace, (2) trigger plus delay ENDS Trace, or (3) Trace EVENTS (store only events that satisfy trigger plus delay conditions). In all three cases the delay can be either clocks or triggers (events).

At the beginning of a Trace cycle, LREST goes low (U24B reset input, Service Sheet 3). This sets Trigger Present Latch U28B (so HTP is low) and clears Data Memory Address Counters U1 and U5.

In STARTS Trace mode (LSTART = low), U1 and U5 are incremented by every qualified external clock (via HWE) after the trigger plus delay specification has been met (reported to memory controller by U15, Service Sheet 3). The occurrence of trigger plus delay is stored in U28B ($\overline{Q}$ output goes high and HTP is now true).

The next 63 states after trigger plus delay are stored in U7 and U16. With storage of the last word HMF goes high. U10B causes memory write pulses (LWE) to be turned off. Also, memory full is reported to the μP.

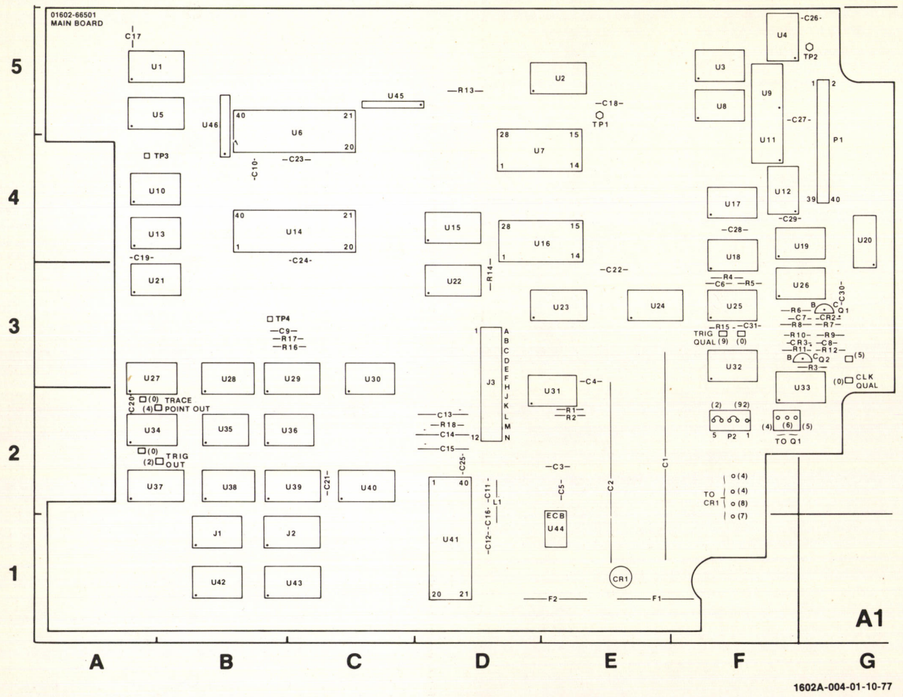
In ENDS Trace mode (LSTART = high), the Trigger Present Latch U28B cannot be set until the memory is full. HMF high sends U10C output high so U15 can report trigger plus delay satisfied. A trigger plus delay event can stop memory fill only if it is the sixty-fourth or greater word captured after Trace is started (via U10C, pin 9).

In store EVENTS Trace mode (HRTE = high), U1 and U5 are allowed to be incremented (by bottom portion of U27) only when a trigger plus delay event occurs.

When the μP polls its trigger present (HTP) and memory full (HMF) bits and finds them both true. the Trace (or Trace Events) is completed.

In the display cycle the μP accesses the Data Memory word desired for display by incrementing the Memory Address Counters (NIMA drives U3A).

TRACE POINT OUT goes low when TRACE key is pressed; it remains low until the trigger plus delay event occurs that starts or ends the Trace in STARTS or ENDS mode. It is set low when LREST goes low (U24B, Service Sheet 3) and returns high when U15 (Service Sheet 3) reports trigger plus delay detected during Trace to U28B.



Main Board A1 Component Locator
(01602-66501)

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	E-2	C15	D-2	C29	F-4	Q1	G-3	R13	D-5	U5	A-5	U19	G-4	U33	G-2
C2	E-2	C16	D-1	C30	G-3	Q2	G-3	R14	D-3	U6	C-5	U20	G-4	U34	A-2
C3	E-2	C17	A-5	C31	F-3	R1	E-2	R15	F-3	U7	D-4	U21	A-3	U35	B-2
C4	E-3	C18	E-5	CR1	E-1	R2	E-2	R16	C-3	U8	F-5	U22	D-3	U36	C-2
C5	E-2	C19	A-4	CR2	G-3	R3	G-3	R17	C-3	U9	F-5	U23	E-3	U37	A-2
C6	F-3	C20	A-2	CR3	F-3	R4	F-3	R18	D-2	U10	A-4	U24	E-3	U38	B-2
C7	G-3	C21	C-2	F1	E-1	R5	F-3	TP1	E-5	U11	F-4	U25	F-3	U39	C-2
C8	G-3	C22	E-3	F2	E-1	R6	F-3	TP2	G-5	U12	F-4	U26	G-3	U40	C-2
C9	B-3	C23	C-4	J1	B-1	R7	G-3	TP3	A-4	U13	A-4	U27	A-3	U41	D-1
C10	B-4	C24	C-4	J2	C-1	R8	F-3	TP4	B-3	U14	C-4	U28	B-3	U42	B-1
C11	D-2	C25	D-2	J3	D-3	R9	G-3	U1	A-5	U15	D-4	U29	C-3	U43	C-1
C12	D-1	C26	G-5	L1	D-2	R10	F-3	U2	E-5	U16	E-4	U30	C-3	U44	E-1
C13	D-2	C27	G-5	P1	G-4	R11	F-3	U3	F-5	U17	F-4	U31	E-2	U45	C-5
C14	D-2	C28	F-4	P2	F-2	R12	G-3	U4	F-5	U18	F-4	U32	F-3	U46	B-5

Figure 8-7. Service Sheet 4, Address Counter and Data Memory (Sheet 1 of 2)

P/O A1 MAIN BOARD ASSY (01602-66501)

IC SUPPLY CONFIGURATIONS

+5V 16 8 U1, 5, 28

+5V 14 7 U3, 8, 10, 13, 21, U27, 34

5 17 LSTART FROM U42E, PIN 10

5 23 HRTE FROM U14, PIN 19

U10A U21A U21E U21F U13B U13A U10C

8 3 TO U15, PIN 4

DATA MEMORY ADDRESS COUNTERS U1/U5

TRACE TRACE EVENTS U27 U21B

U1 U5 LD A B C D ENP ENT >CK CLR QA QB QC QD CARRY OUT NC

U21D

HMF 26 5 TO U6, PIN 38

MA5 MA4 MA3 MA2 MA1 MA0

27 5 TO U6

5 19 NIMA FROM U14, PIN 35

U21C U3A

TP3 +5V C17 22 .01UF +5V

1 FROM POWER SUPPLY

TP4 +12V C23 31 1UF +12V

TRIGGER PRESENT LATCH U28B

3 16 HWE FROM Q2

U8A LWE

TP1

U28B J R Q CK K S

U34B

FROM U15, PIN 9 3 10

3 47 FROM U24B, PIN 10

U10B

HTP 28 5 TO U6, PIN 1

TO U15, PIN 3 9 3

5 22 HSTOP FROM U14, PIN 30

U8C

LSTOP P/O J2 13 TO DISPLAY 41 7

J4 (4) (0) TRACE POINT OUT

16X64 RAM U7 DATA MEMORY U7/U16

16X64 RAM U16

MA5 MA4 MA3 MA2 MA1 MA0 A5 A4 A3 A2 A1 A0

T0 T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13 T14 T15 I0 I1 I2 I3 I4 I5 I6 I7

LWE WE

2 3 3 3 4 3 5 3

5 14 TMU FROM U14, PIN 26

5 15 TML FROM U14, PIN 23

CE

O7 O6 O5 O4 O3 O2 O1 O0 17 18 19 20 21 22 23 24

12 NC 16 NC

U45 R = 4700 8 7 6 5 4 3 2 9

MD7 MD6 MD5 MD4 MD3 MD2 MD1 MD0

TO U6 29 5

ICs ON THIS SCHEMATIC

REF DES	HP PART NO.	MFR PART NO.
U1, 5	1820-1430	AM74LS161N
U3, 27	1820-0691	74S64PC
U7, 16	1816-0728	82S09
U8, 10	1820-0685	SN74S10N
U13	1820-0688	74S20PC
U21	1820-1199	SN74LS04N
U28	1820-1372	74S109DC
U34	1820-0697	74S140PC
U45	1810-0305	1810-0305

PARTS ON THIS SCHEMATIC

P/O A1
C17-31 TP1, 3, 4 U1, 3A, 5, 7, 8A, 8C, 10A, 10B, 10C, 13A, 13B, 16, 21, 27, 28B, 34B, 45

1602A-004-02-10-77

4

Figure 8-7. Service Sheet 4, Address Counter and Data Memory (Sheet 2 of 2)

SERVICE SHEET 5

PRINCIPLES OF OPERATION

The F8 microprocessor CPU (U41) and PSUs (Program Storage Units) U6 and U14 control 1602A data acquisition and data display cycles. In addition, the CPU will perform a program stored in PSU ROM for self-test execution.

The F8 system (CPU and PSUs):

a. Conducts self-test when 1602A is powered on.

b. Reads the keyboard to determine Format and Trace Specification.

c. Loads trigger word into RAM comparators for pattern trigger recognition.

d. Loads delay value into Delay Generator and commands delay by Clocks or Events.

e. Selects clock.

f. Commands Trace mode (Starts, Ends, or Events) to select the data window to be captured by Data Memory (data acquisition).

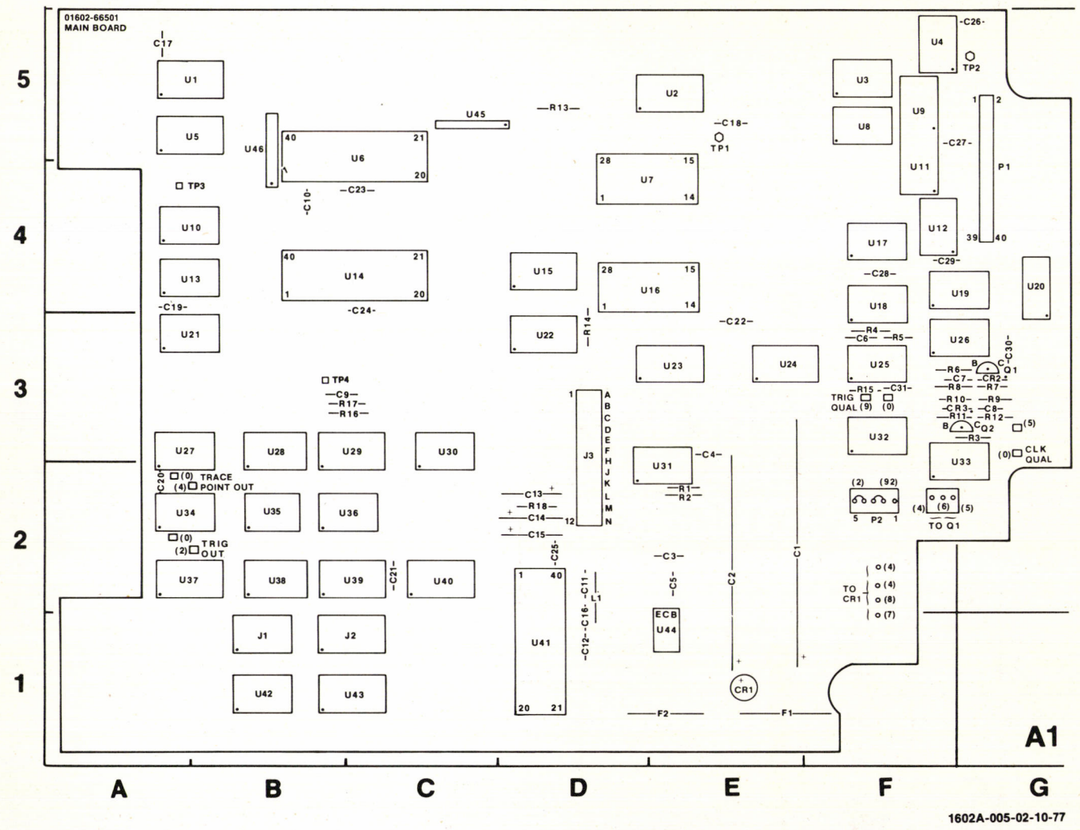
g. Controls display of acquired data (in desired format) during display cycle.

SELF-TEST. Executed each time the 1602A is powered on. The ROMs are check summed, ROM I/O ports are toggled and read back, and RAM is verified (test pattern written and read back).

In addition, data acquisition hardware (with exception of Data Probe A5) is tested. Twenty-two tests are performed on data acquisition hardware to determine its functional operation. Stimulus for these tests is provided by placing Trigger Address Counters/Data Latches (Service Sheet 3) in their count mode. The Clock Switch (Service Sheet 3) is set to the internal 2 MHz μP clock (LST = low).

Each test is started by the μP setting up delay, STARTS/ENDS, and trigger. The test is run and the resulting information in the Data Memory (Service Sheet 4) is compared with a reference in ROM.

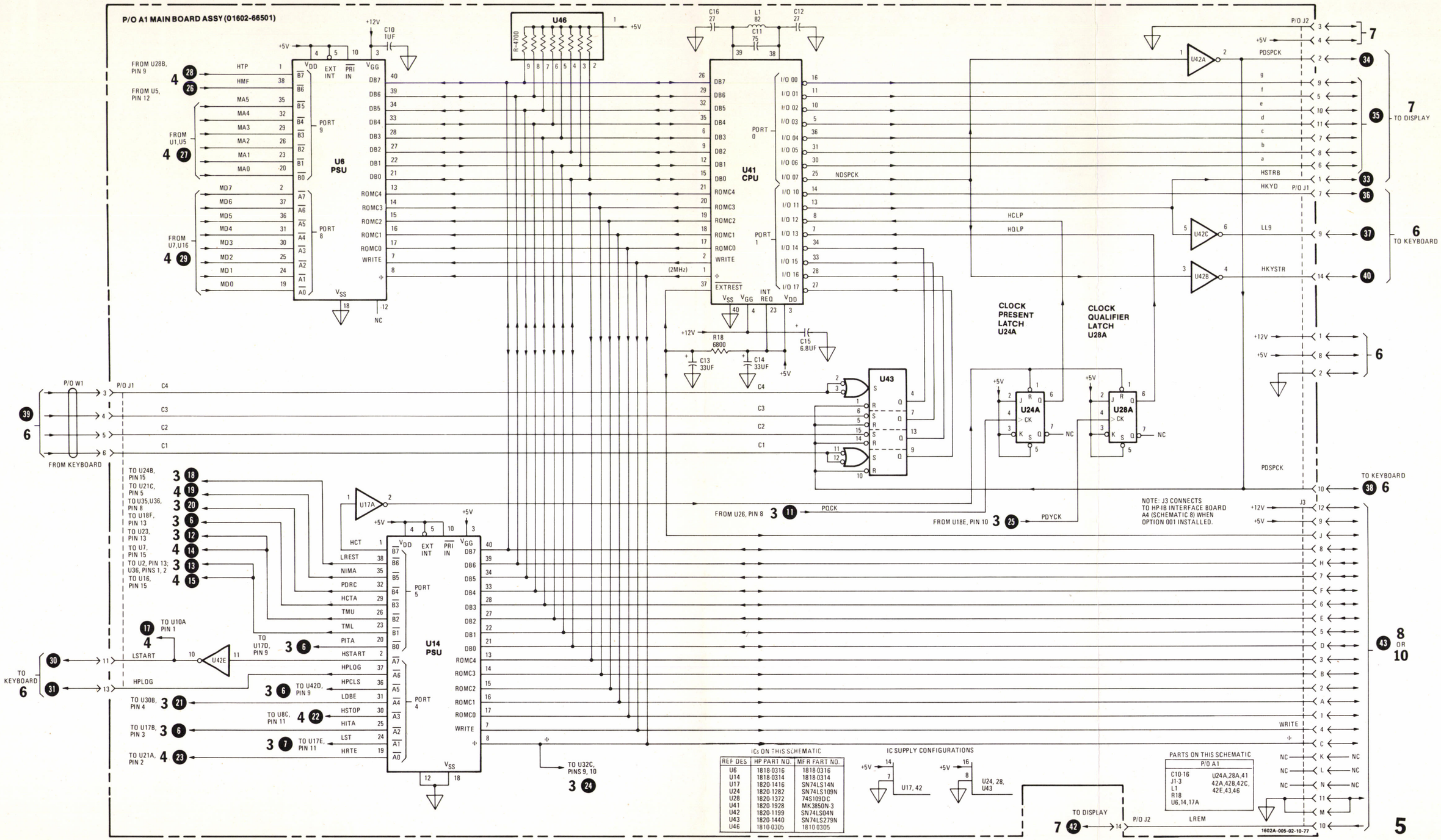
If self-test fails, the message E99 is displayed. Pressing the "d" key causes self-test to repeat and stop on the failed test for diagnosis.



Main Board A1 Component Locator
(01602-66501)

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	E-2	C15	D-2	C29	F-4	Q1	G-3	R13	D-5	U5	A-5	U19	G-4	U33	G-2
C2	E-2	C16	D-1	C30	G-3	Q2	G-3	R14	D-3	U6	C-5	U20	G-4	U34	A-2
C3	E-2	C17	A-5	C31	F-3	R1	E-2	R15	F-3	U7	D-4	U21	A-3	U35	B-2
C4	E-3	C18	E-5	CR1	E-1	R2	E-2	R16	C-3	U8	F-5	U22	D-3	U36	C-2
C5	E-2	C19	A-4	CR2	G-3	R3	G-3	R17	C-3	U9	F-5	U23	E-3	U37	A-2
C6	F-3	C20	A-2	CR3	F-3	R4	F-3	R18	D-2	U10	A-4	U24	E-3	U38	B-2
C7	G-3	C21	C-2	F1	E-1	R5	F-3	TP1	E-5	U11	F-4	U25	F-3	U39	C-2
C8	G-3	C22	E-3	F2	E-1	R6	F-3	TP2	G-5	U12	F-4	U26	G-3	U40	C-2
C9	B-3	C23	C-4	J1	B-1	R7	G-3	TP3	A-4	U13	A-4	U27	A-3	U41	D-1
C10	B-4	C24	C-4	J2	C-1	R8	F-3	TP4	B-3	U14	C-4	U28	B-3	U42	B-1
C11	D-2	C25	D-2	J3	D-3	R9	G-3	U1	A-5	U15	D-4	U29	C-3	U43	C-1
C12	D-1	C26	G-5	L1	D-2	R10	F-3	U2	E-5	U16	E-4	U30	C-3	U44	E-1
C13	D-2	C27	G-5	P1	G-4	R11	F-3	U3	F-5	U17	F-4	U31	E-2	U45	C-5
C14	D-2	C28	F-4	P2	F-2	R12	G-3	U4	F-5	U18	F-4	U32	F-3	U46	B-5

Figure 8-8. Service Sheet 5, Microprocessor and I/O (Sheet 1 of 2)



REF DES	HP PART NO.	MFR PART NO.
U6	1818-0316	1818-0316
U14	1818-0314	1818-0314
U17	1820-1416	SN74LS14N
U24	1820-1282	SN74LS109N
U28	1820-1372	74S109DC
U41	1820-1928	MK3850N-3
U42	1820-1199	SN74LS04N
U43	1820-1440	SN74LS279N
U46	1810-0305	1810-0305

P/O A1	
C10,16	U24A,28A,41
J1-3	42A,42B,42C,
L1	42E,43,46
R18	
U6,14,17A	

Figure 8-8. Service Sheet 5, Microprocessor and I/O (Sheet 2 of 2)

SERVICE SHEET 6

PRINCIPLES OF OPERATION

The 1602A keyboard contains 39 key switches and LED indicators for Logic Polarity, Clock Slope, and Trigger plus Delay Starts or Ends Trace.

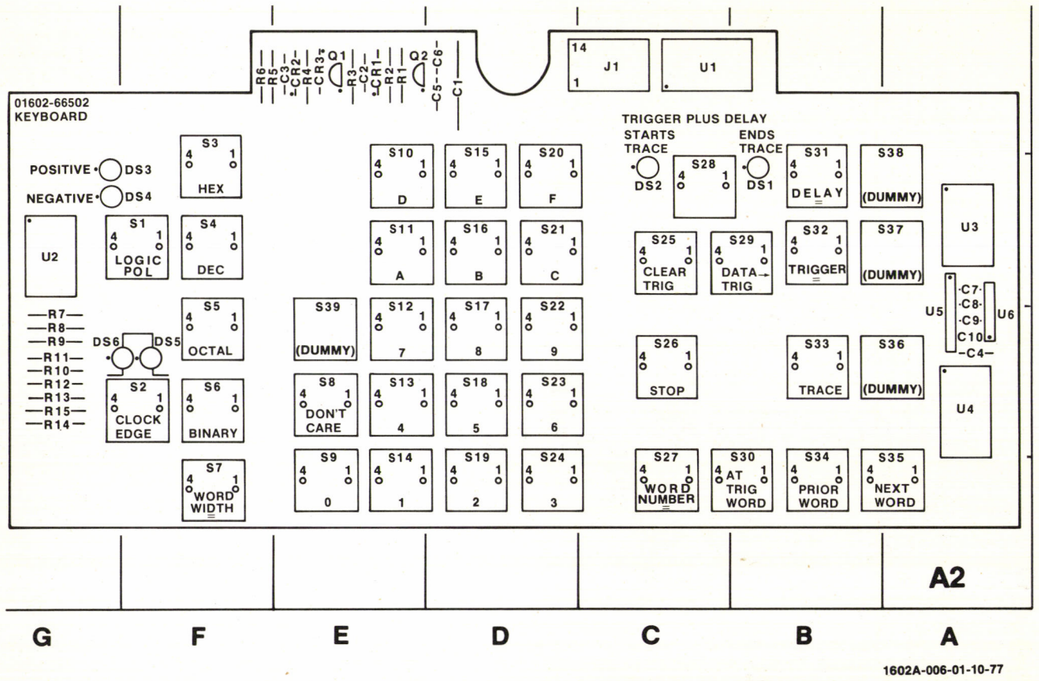
Key switches are wired in a matrix of 9 rows by 4 columns. Each switch has two one-turn coils wrapped around a core. When a key is not pressed, a magnet is held so that its field permeates the core. The core is saturated and there is very little coupling between coils. If the key is pressed, the magnet is released. The core and windings then act as a transformer.

BCD counter U1 selects the row to be driven by BCD-to-decimal decoder U4. At the start of a key scan cycle, LL9 (Low, Load 9) goes low. This sets U1 to a count of 9. LL9 returns high. The next positive edge of PDSPCK sends U1 to a count of 0 and row 0 ("0," "1," "2," and "3" keys) is selected. When PDSPCK goes high, HKYSTR (High, Key Strobe) also goes high. This causes Q1 and Q2 to generate a current ramp that drives the magnetically coupled switches in the selected row.

If a key is down in the row selected by the decoder, flux from the current ramp is coupled from primary to secondary. The column output transistors (Integrators U3Q2-U3Q5) produce a negative-going voltage pulse that is proportional to flux switched in the key switch. U3Q2 thru U3Q5 drive $\overline{R}$ - $\overline{S}$ latches (A1U43, Service Sheet 5). When the processor reads the $\overline{R}$ - $\overline{S}$ latches and finds a key down (an A1U43 Q output is high), it determines key position from column indicated by A1U43 and internal row count.

When a key down is found by the microprocessor, it sets HKYD (High, Key Down) high. This changes the bias point of Integrators U3Q2-U3Q5 because U3Q1 collector voltage decreases. The result of the bias change is a translation downward of the quiescent output level of U3Q2-U3Q5. Less total flux is now required to maintain the negative-going Integrator output pulse. The mechanical hysterisis introduced by HKYD prevents multiple key switch entries (key bounce). When all keys are read in the up position for one scan cycle, HKYD is returned low.

The nine keyboard rows are scanned by the microprocessor during strobing of display characters 2 through 10 (A3U2 to A3U12, Service Sheet 7).



Keyboard A2 Component Locator
(01602-66502)

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	D-4	CR2	E-4	R1	E-4	R11	G-2	S6	F-2	S16	D-3	S26	C-2	R36	A-2
C2	E-4	CR3	E-4	R2	E-4	R12	G-2	S7	F-1	S17	D-2	S27	C-1	R37	A-3
C3	E-4	DS1	B-3	R3	E-4	R13	G-2	S8	E-2	S18	D-2	S28	C-3	R38	A-3
C4	A-2	DS2	C-3	R4	E-4	R14	G-2	S9	E-1	S19	D-1	S29	B-3	R39	E-2
C5	D-4	DS3	G-3	R5	E-4	R15	G-2	S10	E-3	S20	D-3	S30	B-1	U1	C-4
C6	D-4	DS4	G-3	R6	F-4	S1	F-3	S11	E-3	S21	D-3	S31	B-3	U2	G-3
C7	A-3	DS5	F-2	R7	G-2	S2	F-2	S12	E-2	S22	D-2	S32	B-3	U3	A-3
C8	A-3	DS6	G-2	R8	G-2	S3	F-3	S13	E-2	S23	D-2	S33	B-2	U4	A-2
C9	A-2	J1	C-4	R9	G-2	S4	F-3	S14	E-1	S24	D-1	S34	B-1	U5	A-2
C10	A-2	Q1	E-4	R10	G-2	S5	F-2	S15	D-3	S25	C-3	S35	A-1	U6	A-2
CR1	E-4	Q2	E-4												

Figure 8-9. Service Sheet 6, Keyboard A2 (Sheet 1 of 2)

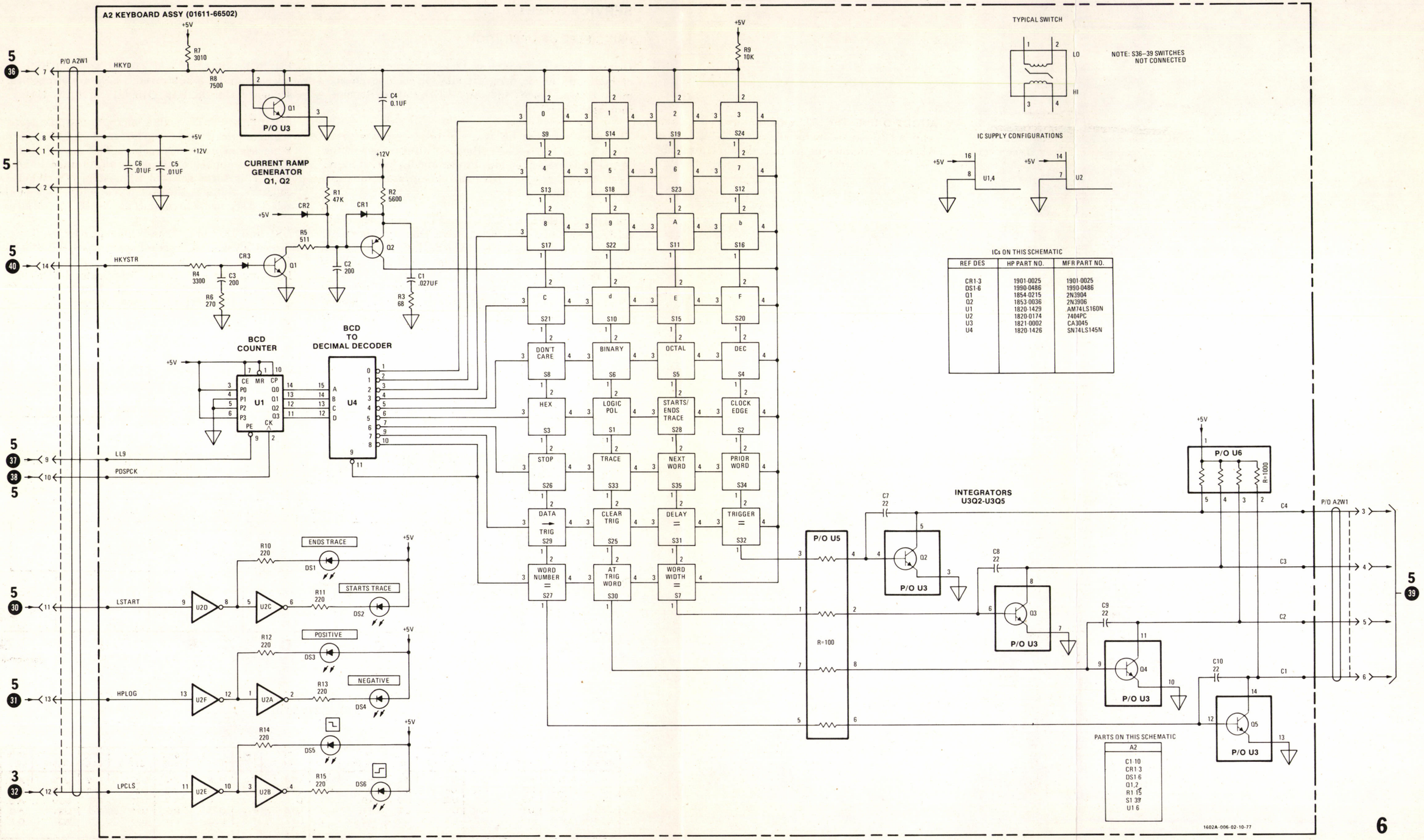


Figure 8-9. Service Sheet 6, Keyboard A2 (Sheet 2 of 2)

SERVICE SHEET 7

PRINCIPLES OF OPERATION

Display Board A3 contains 18 seven-segment LEDs, cathode and anode drive circuits for each seven-segment LED, "Trace" indicator LEDs, and "Remote" indicator LEDs.

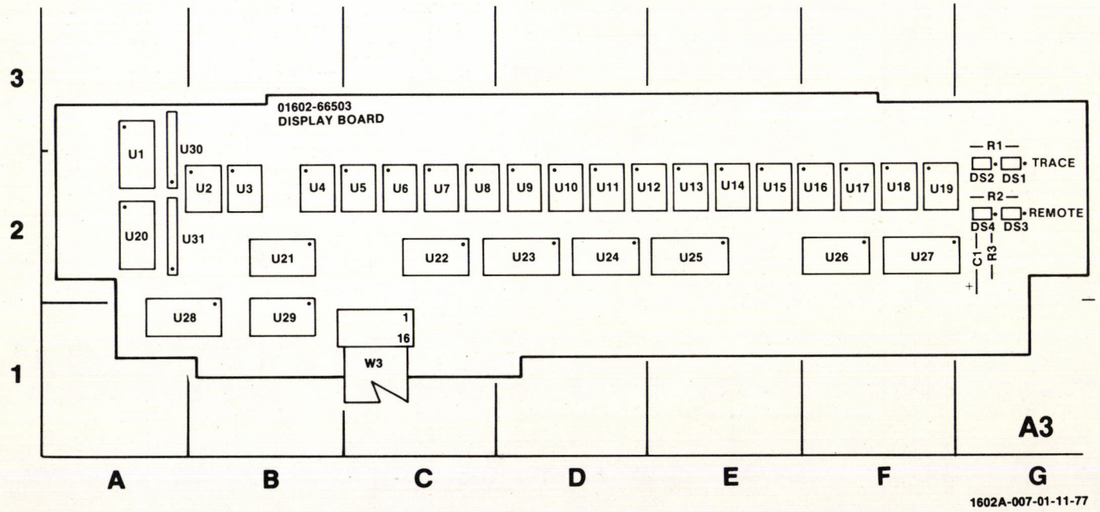
The seven-segment LEDs are strobed one at a time. When an LED is strobed, cathodes of all seven segments in the LED are driven low. Proper anodes are set high. Desired segments turn ON to display information sent from the microprocessor.

CATHODE DRIVE. U23, U25, and U27 are clocked by positive edge of PDSPCK (Positive, Display Clock). At the start of a display cycle, HSTRB (High, Strobe) goes high for approximately one display clock period. This high is applied to U23 pin 13 (D input) and clocked through to U23 pin 12 (Q output) by PDSPCK. U23 pin 12 high is inverted by U22D. This drives U3 cathodes low (U3 strobed). HSTRB goes low, and the next PDSPCK sends U23 pin 12 low, U23 pin 10 high. U3 is released and U2 is strobed. LEDs are strobed in the sequence: U3, U2, U19, U18, U17, U16, . . . U4.

ANODE DRIVE. The 1602A microprocessor sets selected segment lines (a through g) high as each LED is strobed. When segment lines are set high, they are inverted (U21, U29) and applied to transistors contained in U1 and U20. This turns selected transistors ON. When ON, collector voltages go high (Vce → 0). This enables selected segments to conduct on the LED being strobed.

DS1 and DS2 are "Trace" indicator LEDs. They are turned ON while a Trace is in progress (L STOP is high).

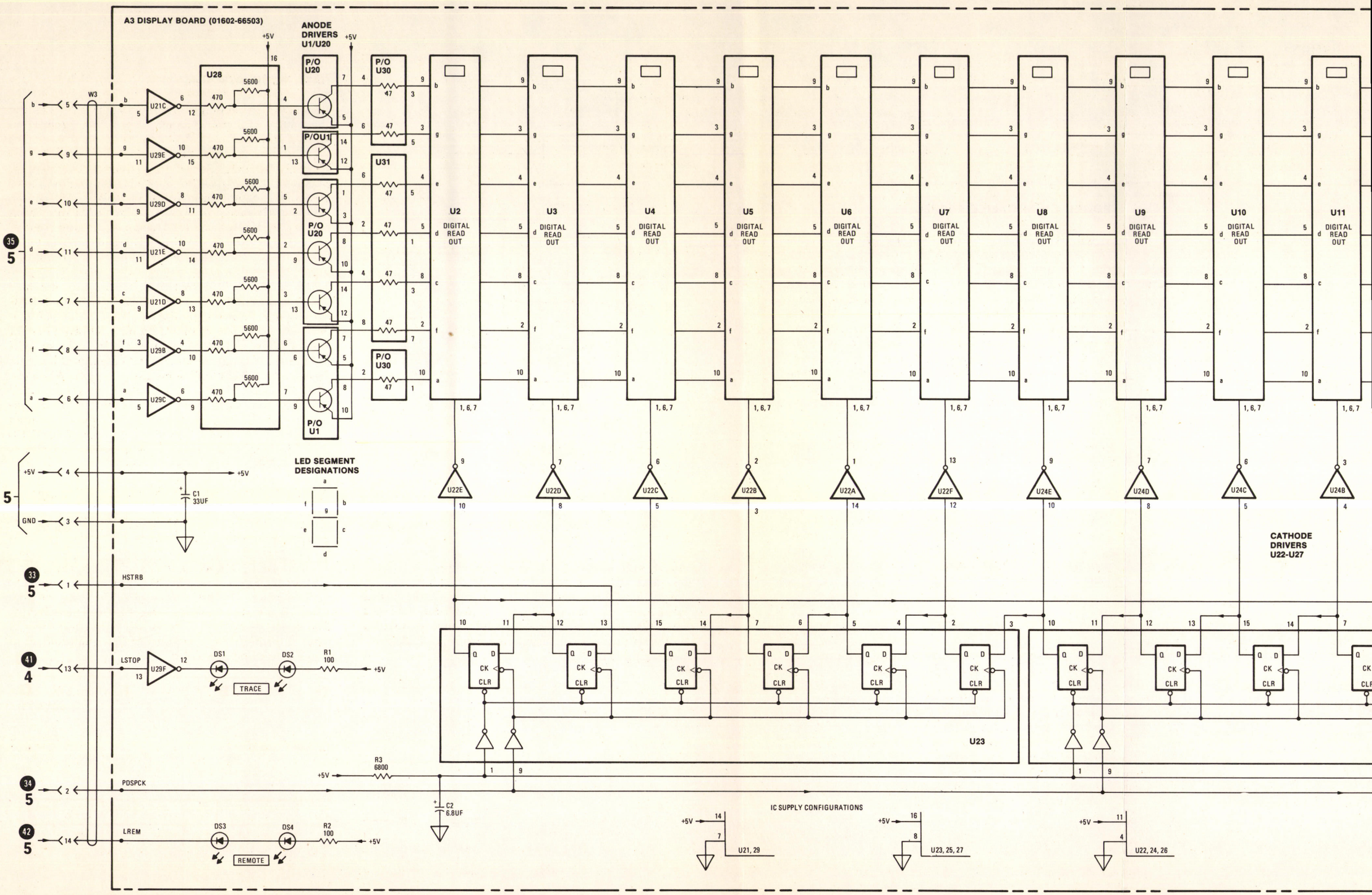
DS3 and DS4 are "Remote" indicator LEDs. Remote operation is possible only when Option 001 (HP-IB) is installed. LREM (Low, Remote) goes low to turn DS3 and DS4 ON.

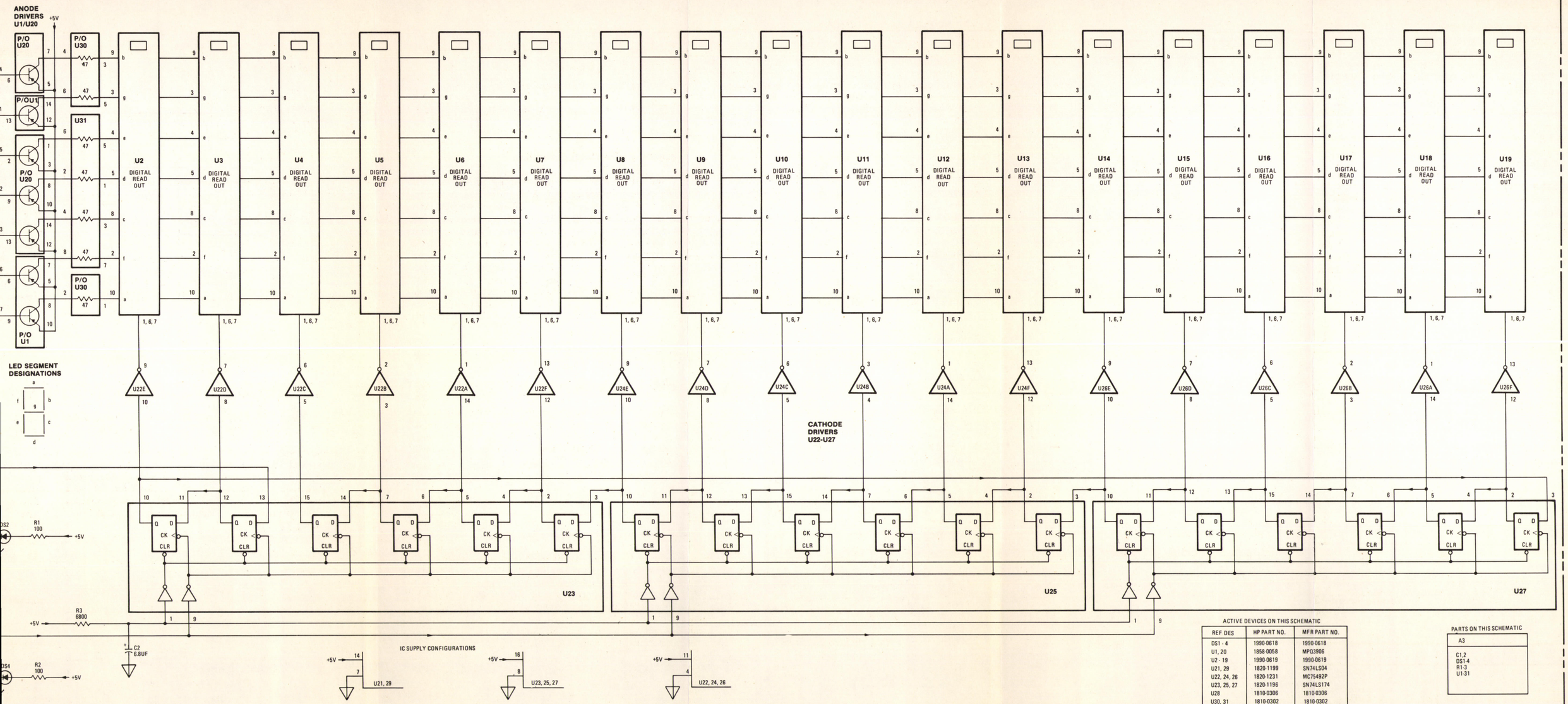


Display Board A3, Component Locator
(01602-66503)

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	G-2	R1	G-3	U3	B-2	U8	C-2	U13	E-2	U18	F-2	U23	D-2	U28	A-1
DS1	G-2	R2	G-2	U4	B-2	U9	D-2	U14	E-2	U19	F-2	U24	D-2	U29	B-1
DS2	G-2	R3	G-2	U5	C-2	U10	D-2	U15	E-2	U20	A-2	U25	E-2	U30	A-3
DS3	G-2	U1	A-2	U6	C-2	U11	D-2	U16	F-2	U21	B-2	U26	F-2	U31	A-2
DS4	G-2	U2	B-2	U7	C-2	U12	D-2	U17	F-2	U22	C-2	U27	F-2	W3	C-1

Figure 8-10. Service Sheet 7, Display Board A3 (Sheet 1 of 2)


A3 DISPLAY BOARD (01602-66503)
ANODE DRIVERS U1/U20
+5V
W3
U28
5600
470
U21C
U29E
U29D
U21E
U21D
U29B
U29C
P/O U20
P/OU1
P/O U30
U31
P/O U1
47
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
DIGITAL READ OUT
1, 6, 7
U22E
U22D
U22C
U22B
U22A
U22F
U24E
U24D
U24C
U24B
CATHODE DRIVERS U22-U27
LED SEGMENT DESIGNATIONS
a
b
c
d
e
f
g
+5V
GND
C1 33UF
HSTRB
LSTOP
U29F
DS1
DS2
TRACE
R1 100
PDSPCK
R3 6800
C2 6.8UF
LREM
DS3
DS4
REMOTE
R2 100
Q D
CK
CLR
U23
IC SUPPLY CONFIGURATIONS
U21, 29
U23, 25, 27
U22, 24, 26



ACTIVE DEVICES ON THIS SCHEMATIC

REF DES	HP PART NO.	MFR PART NO.
DS1 - 4	1990-0618	1990-0618
U1, 20	1858-0058	MPQ3906
U2 - 19	1990-0619	1990-0619
U21, 29	1820-1199	SN74LS04
U22, 24, 26	1820-1231	MC75492P
U23, 25, 27	1820-1196	SN74LS174
U28	1810-0306	1810-0306
U30, 31	1810-0302	1810-0302

PARTS ON THIS SCHEMATIC

A3
C1,2 DS1-4 R1-3 U1-31

1602A-007-02-11-77

7

Figure 8-10. Service Sheet 7, Display Board A3 (Sheet 2 of 2)

SERVICE SHEET 8

PRINCIPLES OF OPERATION

The Hewlett-Packard Interface Bus circuits (Option 001) add listener/talker capability to the 1602A. When a listener, it receives commands via HP-IB that simulate front panel key entries for measurement setup and execution. When a talker, it outputs measurement status or results. For additional information, refer to IEE Std. 488-1975 "Standard Digital Interface for Programmable Instrumentation."

Bus Mnemonics: (HP-IB is Low = True Logic)

DI01-DI08 ..... Data Input/Output
EOI ..... End Or Identify
DAV ..... Data Valid
NRFD ..... Not Ready for Data
NDAC ..... Data Not Accepted
IFC ..... Interface Clear
SRQ ..... Service Request
ATN ..... Attention
REN ..... Remote Enable

HP-IB DATA TRANSFER (Handshake).

1. NRFD goes high (wired-and; all listeners are ready for data).

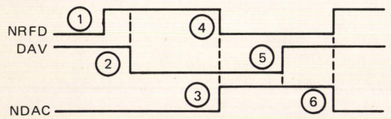
2. DAV goes low (talker says data on DIO lines is valid).

3. NDAC goes high (wired-and; all listeners have accepted the data).

4. Listener can set NRFD back to low as soon as DAV goes low, NRFD must go low before or at same time as NDAC goes high.

5. Talker can set DAV high after NDAC goes high.

6. Listener can set NDAC back to low as soon as DAV goes high. NDAC must go low before or at same time as NRFD goes high.



Handshake Sequence

Operation of HP-IB Interface Board A4 is covered by three cases:

a. Power-on initialize and IFC.

b. HP-IB in Command Mode (ATN low).

c. HP-IB in Data Mode (ATN high).

POWER-ON INITIALIZE AND IFC.

When HP-IB PSU (Program Storage Unit) U9 sends LPON (low, Power on) low, A4 is initialized. ACK flip-flop U2A and Ready flip-flop U2B are pre-set, Talk and Listen flip-flops (U20B/U20A) are cleared, and $\overline{S}$-$\overline{R}$ latch U3C (Part of Remote/Local State Machine) output is set high. U2B signals U9 and U14C that the 1602A is ready to participate in Handshakes. With U20B and U20A Q outputs both low, the 1602A cannot "listen" or "talk." It must now receive its listen or talk address (while bus is in the Command Mode) in order to become a "listener" or a "talker." U3C output high prevents local lockout (Return to Local Key disable) when A4 is initialized.

When a Controller is turned on, it sends IFC low. This clears 1602A Talk and Listen flip-flops.

COMMAND MODE (ATN low).

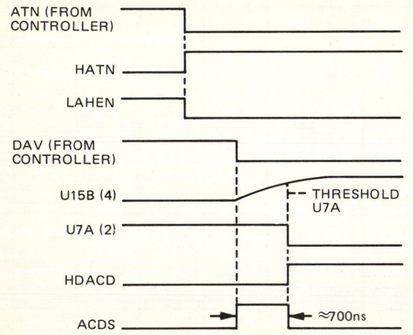
When ATN is driven low by the Controller, the 1602A will respond to; (a) its listen address, (b) its talk address, (c) a universal unlisten command, (d) a go to local command (if previously addressed to listen), (e) a local lock out command, (f) IFC, or (g) REN.

NOTE

1602A will respond to IFC and REN inputs in either Command or Data mode.

Source Handshake is disabled (U4A output high). Acceptor Handshake is enabled (U15C output low). Decoder U5A is enabled so 1602A can determine whether Controller is generating a listen or talk address. Decoder U5B enables part of decoder U6 when ATN is low and ACDS (Accept Data State) is high. U6 allows 1602A to receive "go to local" or "local lock out" commands (determined by code of LD0-LD6).

ACDS pulse generation is shown in the following timing diagram:



ACDS Pulse Generation

Positive edge of ACDS latches 1602A into "talk," "listen," or "unlisten," depending on information sent by Controller. DIO lines 1 thru 5 (LD0-LD4) are compared to 1602A address switch by comparator U18. If a match is determined, then the 1602A is placed in "talk" or "listen" according to information sent on DIO lines 6 and 7 (LD5 and LD6).

ACDS high sets 1602A to Remote operation if REN is low and 1602A is receiving its listen address. U3A output goes low when 1602A is in Remote (keyboard ignored except Return to Local key). U3A output is sent via U9 to 1602A microprocessor for Remote command implementation. U3A output also turns on 1602A front-panel REMOTE light.

DATA MODE (ATN high).

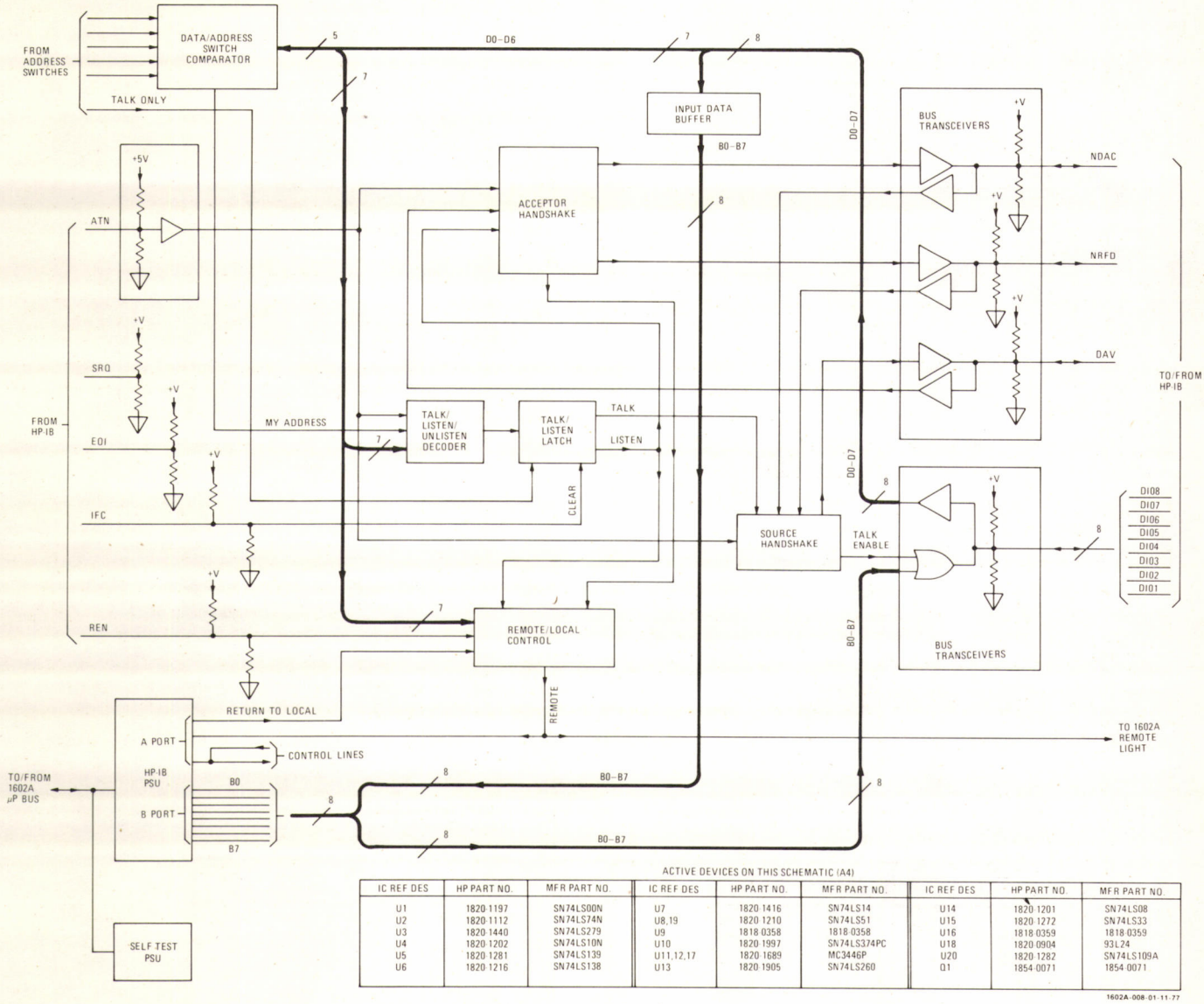
Depending on commands received while ATN was low, the 1602A will now "listen," "talk," or ignore bus conversations.

When a "listener," Source Handshake is disabled. Q1 requires 1602A to be in Remote for incoming data to be accepted. Acceptor handshake is enabled (U15C output low). Positive edge of ACDS latches data into input buffer U10. U5B causes U2B to stop signalling "ready" when ACDS and ATN are high. U9 reads U10 contents, then clocks U2B to release the "not ready" condition.

When a "talker," Acceptor Handshake is disabled (U15C output high). This sets 1602A NRFD and NDAC outputs high. Source Handshake is enabled (U4A output low). U9 places output data on LB0-LB7 lines for transmission on DI01-DI08 lines. U9 then clocks ACK flip-flop U2A Q output high to indicate that it has talk data ready (1602A has something to say). When listener(s) signal ready (NRFD input goes high) and LDAVD (Low, Data Valid Drive) is high, U15D output voltage increases as C3 charges. When U7C input threshold is reached (approximately 3 μs after NRFD went high) its output goes low, which sets LDAVD low and 1602A DAV output is now low.

When DAV goes low, U15A sends HDACD high. Listeners signal acceptance of the transmitted byte by setting NDAC high. NDAC and HDAVD high cause ACK flip-flop U2A to be cleared.

With HDACD, NDAC, and U2A $\overline{Q}$ high, the bottom portion of U8B causes LDAVD to be returned high. The upper portion of U8B allows LDAVD to be set high when 1602A transmission is interrupted. The ACK flip-flop is not affected. The 1602A will retransmit the byte after the interruption is over so that the handshake sequence can be completed.

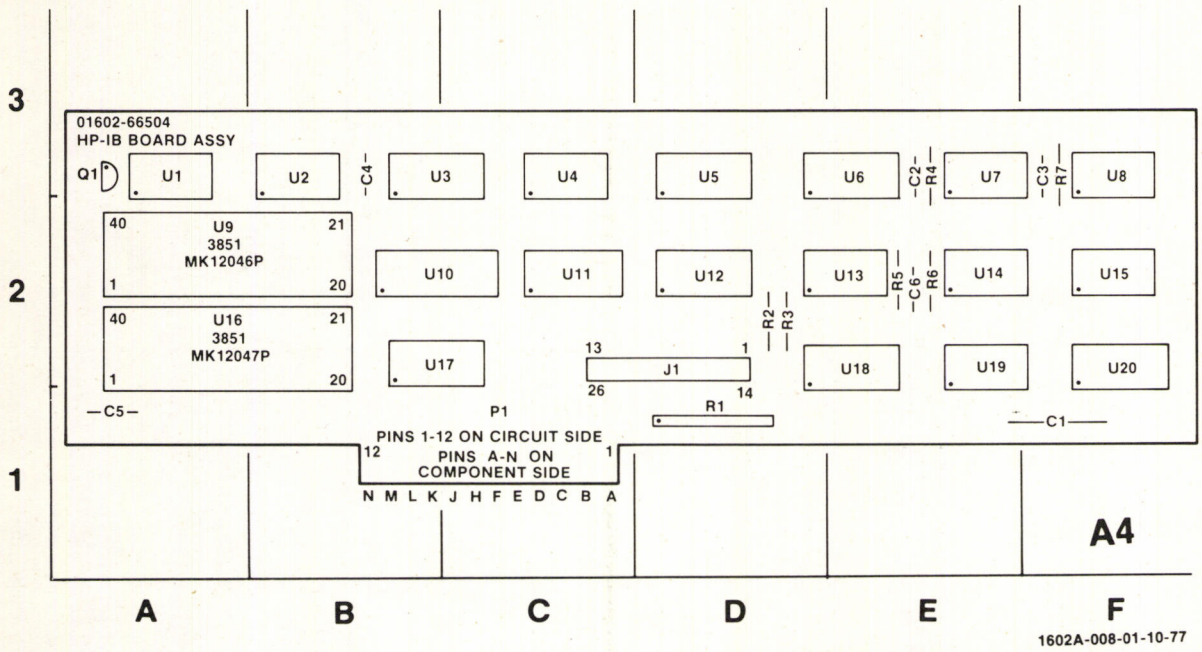


ACTIVE DEVICES ON THIS SCHEMATIC (A4)

IC REF DES	HP PART NO.	MFR PART NO.	IC REF DES	HP PART NO.	MFR PART NO.	IC REF DES	HP PART NO.	MFR PART NO.
U1	1820-1197	SN74LS00N	U7	1820-1416	SN74LS14	U14	1820-1201	SN74LS08
U2	1820-1112	SN74LS74N	U8,19	1820-1210	SN74LS51	U15	1820-1272	SN74LS33
U3	1820-1440	SN74LS279	U9	1818-0358	1818-0358	U16	1818-0359	1818-0359
U4	1820-1202	SN74LS10N	U10	1820-1997	SN74LS374PC	U18	1820-0904	93L24
U5	1820-1281	SN74LS139	U11,12,17	1820-1689	MC3446P	U20	1820-1282	SN74LS109A
U6	1820-1216	SN74LS138	U13	1820-1905	SN74LS260	Q1	1854-0071	1854-0071

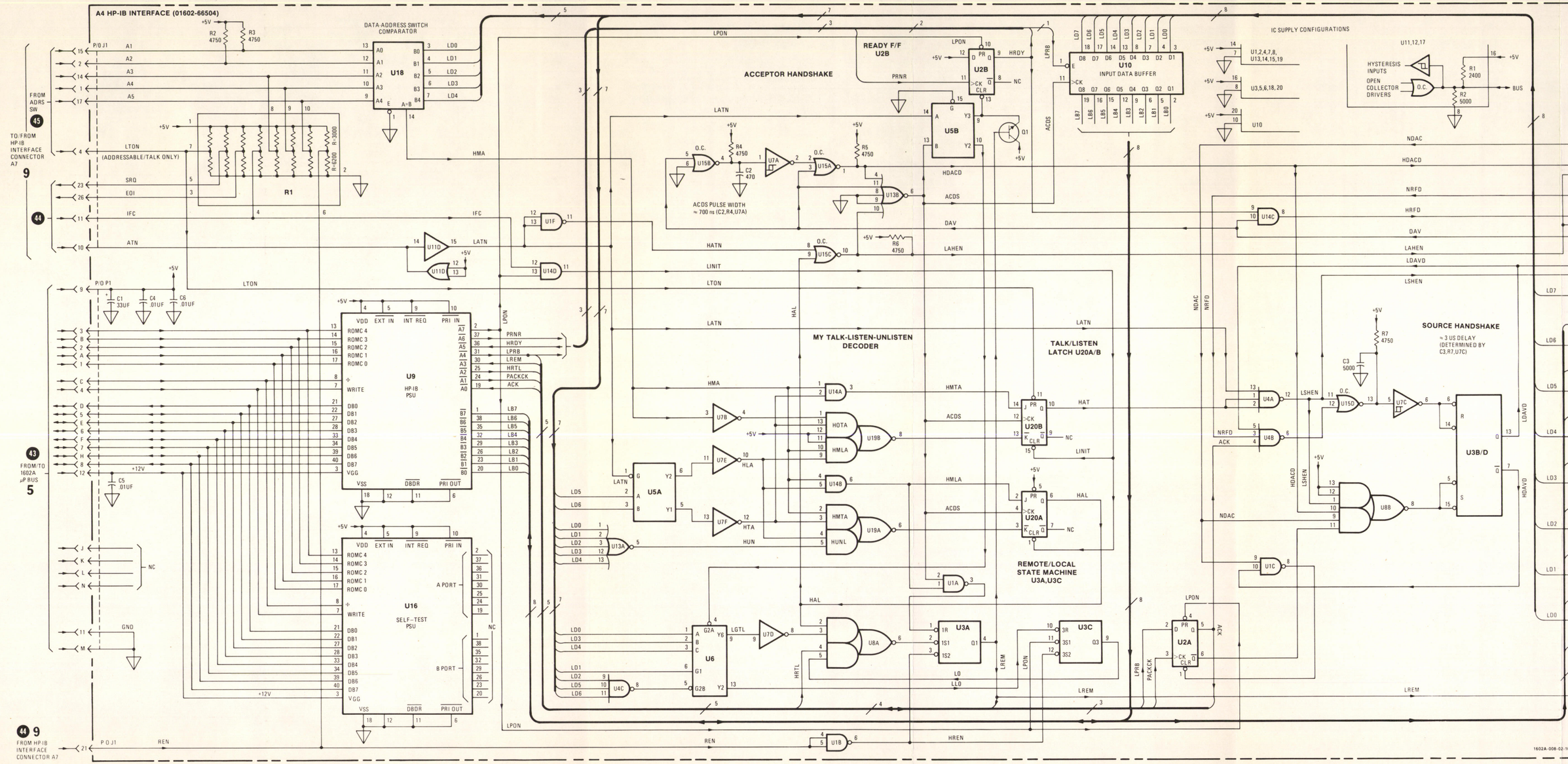
HP-IB Interface Board A4 Block Diagram

Figure 8-11. Service Sheet 8, HP-IB Interface Board A4 (Sheet 1 of 2)



HP-IB Interface Board A4 Component Locator
(01602-66504)

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	F-1	F1	D-2	R4	E-3	U3	C-3	U9	A-2	U15	F-2
C2	E-3	Q1	A-3	R5	E-2	U4	C-3	U10	C-2	U16	A-2
C3	F-3	P1	C-1	R6	E-2	U5	D-3	U11	C-2	U17	C-2
C4	B-3	R1	D-1	R7	F-3	U6	E-3	U12	D-2	U18	E-2
C5	A-1	R2	D-2	U1	A-3	U7	E-3	U13	E-2	U19	E-2
C6	E-2	R3	D-2	U2	B-3	U8	F-3	U14	E-2	U20	F-2


A4 HP-IB INTERFACE (01602-66504)
DATA-ADDRESS SWITCH COMPARATOR
U18
FROM ADRS SW
TO/FROM HP-IB INTERFACE CONNECTOR A7
LTON
(ADDRESSABLE/TALK ONLY)
SRQ
EOI
IFC
ATN
R1
R-3000
R-6200
FROM/TO 1602A μP BUS
U9
HP-IB PSU
U16
SELF-TEST PSU
U6
U5A
U5B
READY F/F U2B
ACCEPTOR HANDSHAKE
ACDS PULSE WIDTH ≈ 700 ns (C2,R4,U7A)
MY TALK-LISTEN-UNLISTEN DECODER
TALK/LISTEN LATCH U20A/B
REMOTE/LOCAL STATE MACHINE U3A,U3C
INPUT DATA BUFFER
U10
IC SUPPLY CONFIGURATIONS
U11,12,17
U1,2,4,7,8, U13,14,15,19
U3,5,6,18,20
HYSTERESIS INPUTS
OPEN COLLECTOR DRIVERS
SOURCE HANDSHAKE
≈ 3 US DELAY (DETERMINED BY C3,R7,U7C)
U3B/D
FROM HP-IB INTERFACE CONNECTOR A7
REN
1602A-008-02-N

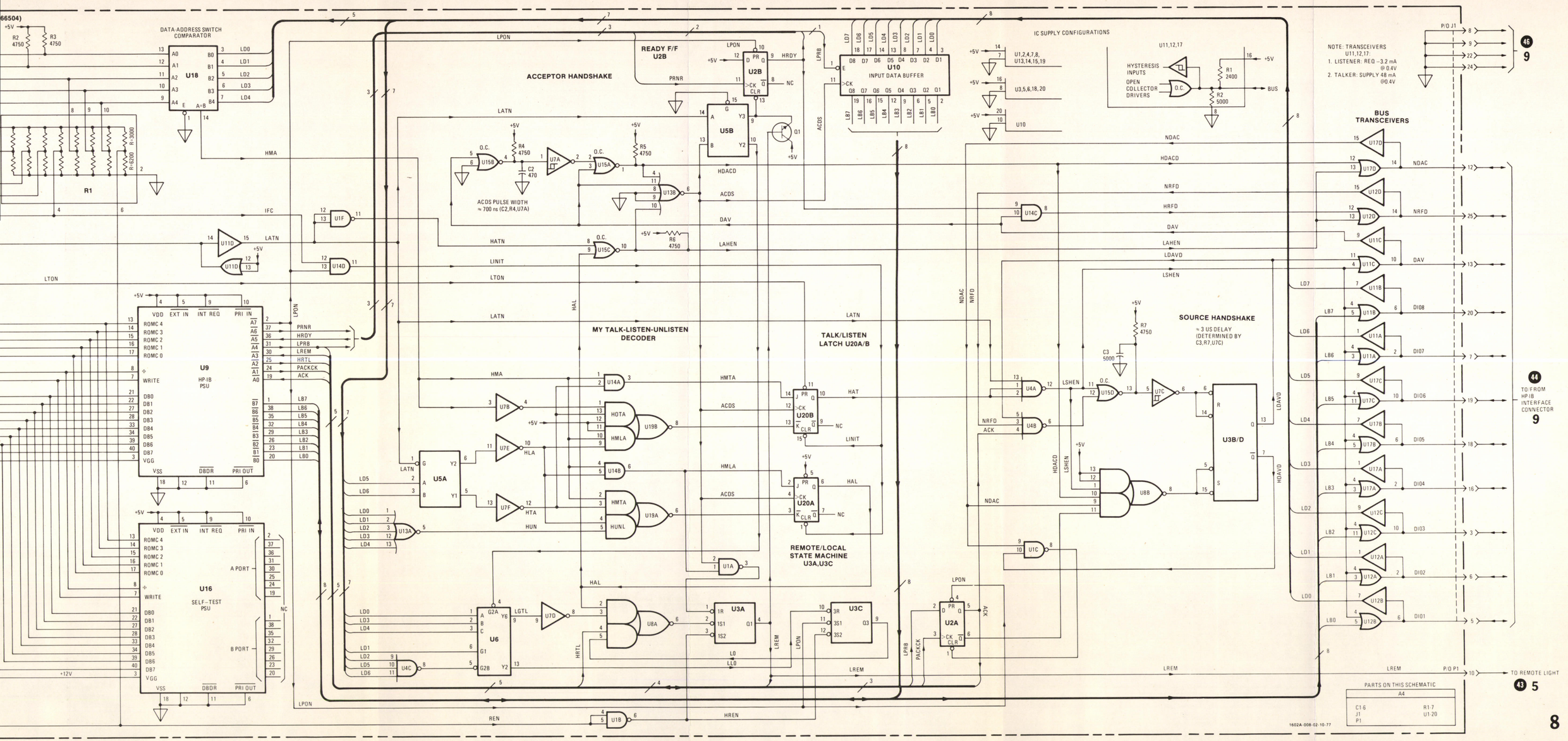


Figure 8-11. Service Sheet 8, HP-IB Interface Board A4 (Sheet 2 of 2)

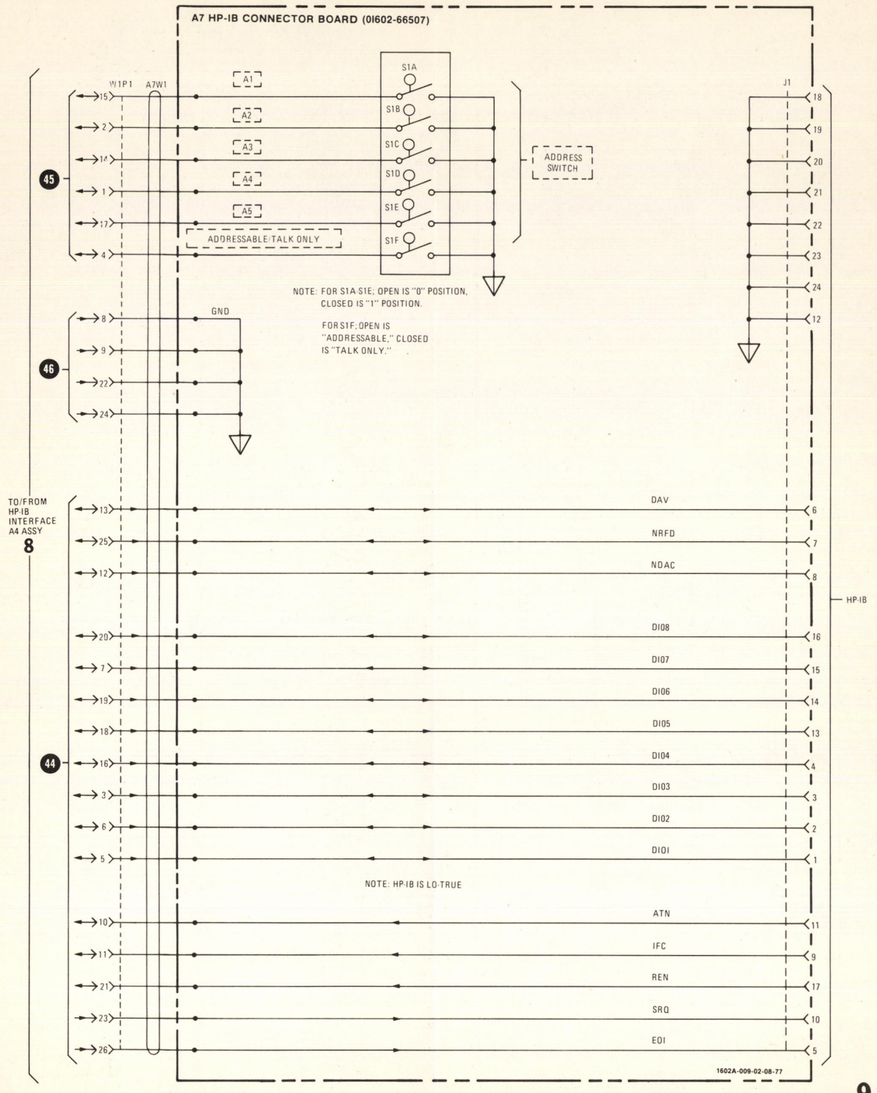
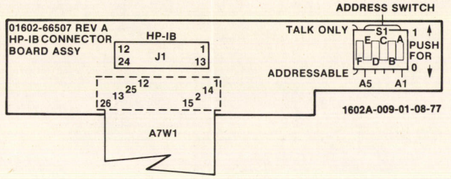


Figure 8-12. P/O Service Sheet 9, HP-IB Connector Board A7

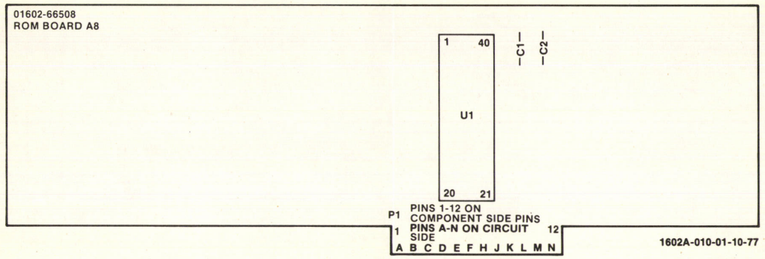
NOTE: HP-IB Connector Board A7 only present when Option 001 installed



HP-IB Connector Board A7 Component Locator
(01602-66507)

Figure 8-12. P/O Service Sheet 9

NOTE: ROM Board A8 replaced by HP-IB Interface Board A4 (Service Sheet 8) when Option 001 installed.



ROM Board A8 Component Locator
(01602-66508)

Figure 8-13. P/O Service Sheet 10

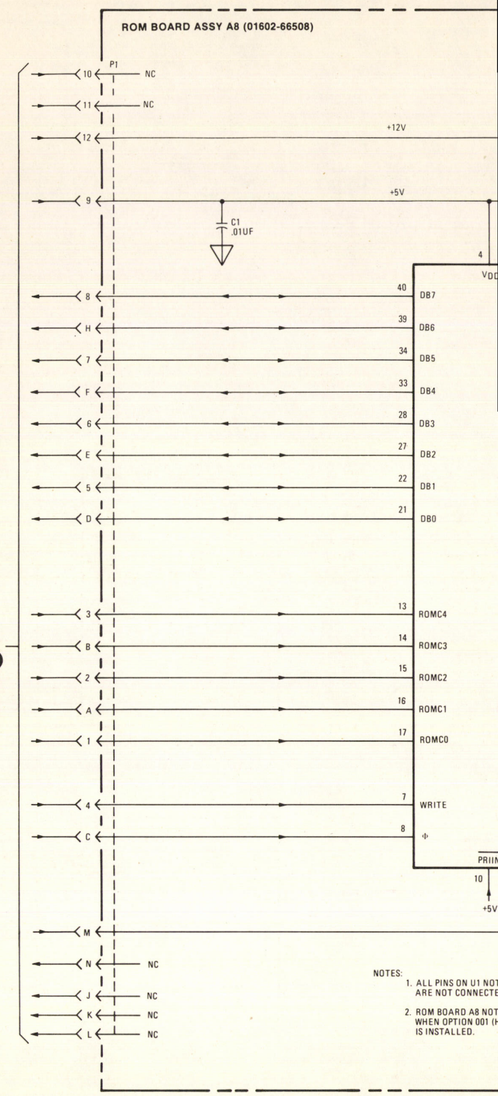
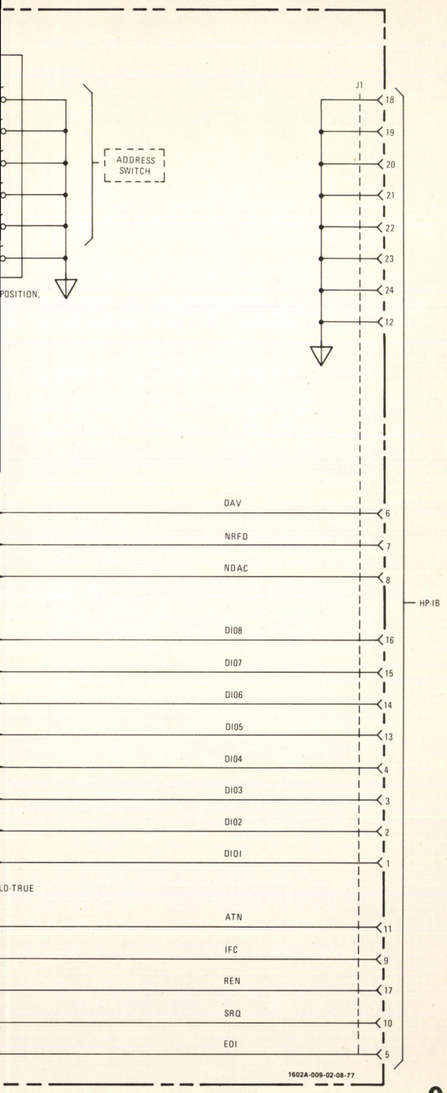


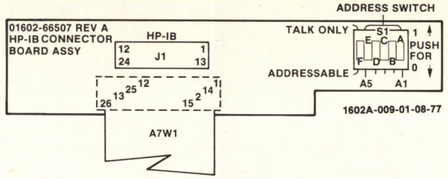
Figure 8-13. P/O Service Sheet 10, R



9

9, HP-IB Connector Board A7

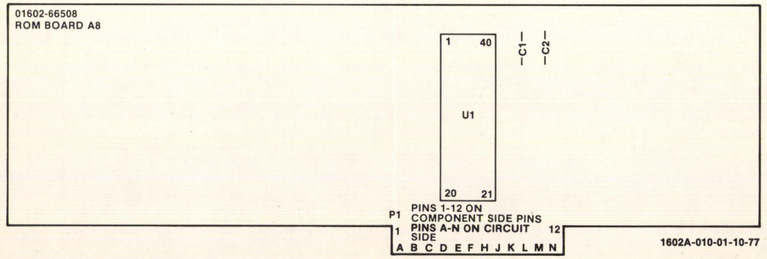
NOTE: HP-IB Connector Board A7 only present when Option 001 installed



HP-IB Connector Board A7 Component Locator
(01602-66507)

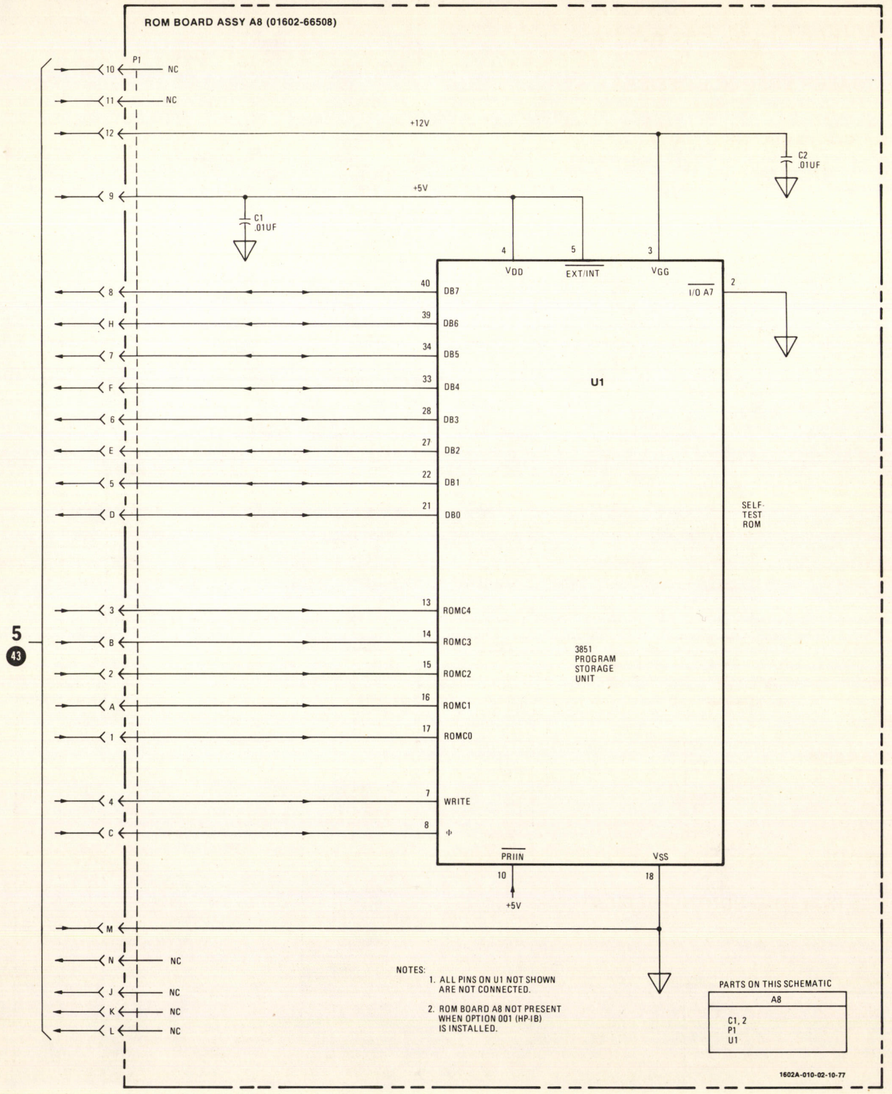
Figure 8-12. P/O Service Sheet 9

NOTE: ROM Board A8 replaced by HP-IB Interface Board A4 (Service Sheet 8) when Option 001 installed.



ROM Board A8 Component Locator
(01602-66508)

Figure 8-13. P/O Service Sheet 10



5
43

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Figure 8-13. P/O Service Sheet 10, ROM Board A8

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Telex: 011-3751
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